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ADVANCED LOW COST UNIVERSAL 20 GHz MONOLITHIC RECEIVER FRONT-END

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FORWARD

This is the final report for contract NAS3-24894 with NASA Lewis Research Center, "Advanced Low-Cost Universal 20 GHz Monolithic Receiver Front-End", covering the period from April 24, 1986 to April 23, 1988. Dr. D.R. Ch'en was the program manager for this effort, and was responsible for the fabrication of the receiver front-end monolithic chips. Dr. W.C. Petersen was the principal investigator for this effort, and in conjunction with Dr. D.P. Siu was responsible for the design and characterization of the monolithic circuits. Mr. R.D. Fairman was responsible for materials qualification and preparation. Mr. G. Fujikawa was the NASA technical monitor for the entire activity.

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1) INTRODUCTION

A key to the development of affordable ground terminals for advanced 20/30 GHz satellite communications systems, such as those spearheaded by NASA, is the development of a low cost front-end which converts the in-coming RF signal to an intermediate frequency for further processing. Current technology is based extensively on hybrid circuit techniques, where each component consists of several Microwave Integrated Circuit (MIC) modules. However, the costly individual assembly and tuning required to produce this type of component has already been highly optimized, therefore current high unit costs are not expected to decline substantially under high volume production. In a multi-phase program, Microwave Monolithics Incorporated (MMInc.) is developing a receiver front end based on extensive use of Monolithic Microwave Integrated Circuit (MMIC) technology to circumvent these difficulties and thus dramatically reduce the ultimate production costs of 20/30 GHz ground terminals.

Keeping the goal of low production costs firmly in mind, MMInc.'s design approach utilizes MMICs only for those functions which make economic sense. Thus, the receiver front end incorporates a high performance hybrid first stage to set the system noise floor followed by a high gain monolithic 20 GHz amplifier. Discrete filters are retained due to their lower costs and higher performance. Integration levels are similarly guided by economics rather than aesthetics. Therefore the remainder of the receiver front-end consists of two additional MMICs; a mixer / intermediate frequency amplifier MMIC provides the actual down conversion and additional gain, while a dielectrically stabilized local oscillator MMIC provides the reference signal necessary for down conversion to the IF band. Due to the commercial availability of 3.7 to 4.2 GHz Television Receive Only (TVRO) downconverters at extremely attractive prices, this band has been selected as the IF frequency for MMInc.'s 20 GHz downconverter. Selection of this IF band virtually assures that the remainder of the 20 GHz receiver could be designed and procured at low cost.

This report covers phase II of the the receiver development effort, in which proof of concept has been demonstrated. The preliminary MMIC chip designs for the LNA and DSO from program phase I were finalized, and the design of the mixer and IF amplifier were initiated and completed. The bulk of the program effort then centered on the fabrication and design iteration of these chips. An executive summary is provided in section 2. This is followed by a detailed description of the receiver front end MMICs in section 3. Fabrication techniques utilized for these high performance MMICs are described in section 4, and measured performance of the monolithic receiver front-end components are presented in sections 5 and 6. (A description of the circuit test configurations used in these measurements is provided in Appendix A). High volume production cost estimates of the MMIC chips are summarized in section 7, while section 8 contains a discussion of the changes necessary for operation at alternate IF frequencies such as those utilized in the the Advanced Communications Technology Satellite (ACTS) developed by NASA. Conclusions and recommendations for future work are presented in section 9.

2) EXECUTIVE SUMMARY

This is the final report for contract No. NAS3-24894 with NASA Lewis Research Center, covering phase II of a multi phase program to develop an "Advanced Low-Cost Universal 20 GHz Monolithic Receiver Front-End". Such low cost receivers are urgently needed to realize the full potential of the 30/20 GHz satellite communications systems being developed by NASA, and could prove vital even to the full scale testing of experimental satellite systems. Although current receiver technology can meet the performance requirements, low cost production is a crucial but elusive requirement for the ultimate wide scale utilization of this emerging technology.

Microwave Monolithics Incorporated (MMInc.) has proposed to make both the technical and cost goals for the satellite receiver attainable by developing a monolithic GaAs chip set for the currently high cost receiver front end. This chip set consists of a 20 GHz low noise amplifier (LNA), a dielectrically stabilized local oscillator (DSO), and a mixer / intermediate frequency amplifier (MXR/IFA). In addition to implementing the down converter in Monolithic Microwave Integrated Circuit (MMIC) form to minimize ultimate production costs, several unique features of this chip set design approach further help to minimize ultimate production costs of the receiver. Two aspects of MMInc.'s design approach are particularly noteworthy: 1) The provision for a single stage hybrid amplifier at the waveguide / downconverter interface, and 2) Selection of the high volume low cost Television Receive Only (TVRO) RF band as the first IF frequency of the 20 GHz receiver. The former relaxes performance requirements of the monolithic LNA for enhanced yields and reduced cost while also allowing individualized downconverter tuning in the low loss waveguide transmission medium to maximize performance. Due to the extremely low cost of existing commercially available TVRO downconverters (and indeed entire receivers), selection of the 3.7 to 4.2 GHz frequency range for the first IF frequency virtually assures that the remainder of the 20 GHz receiver could be designed and procured at low cost.

In this phase of the program, the preliminary chip designs from program phase I for the LNA and DSO were finalized, and the design of the mixer and IF amplifier were initiated and completed. Following several iterations of fabrication, characterization, modification, and re-characterization, impressive performance results have been obtained. Over 20 dB gain has been measured from the single chip LNA over the full 17.7 to 20.2 GHz RF band, and high gain is actually available from low Ku-Band frequencies to above 22 GHz. This measured performance is fully compatible with the originally proposed systems approach. The DSO MMIC developed under this program has demonstrated a negative resistance region across the full 14 to 16 GHz range necessary to selectively map the 17.7 to 20.2 GHz RF input band into the 3.7 to 4.2 GHz band. Thus this single MMIC design can be utilized for any desired sub-band by simply selecting the appropriate dielectric resonator. Locking to a dielectric resonator has been demonstrated during this program by the fabrication, characterization, and delivery to NASA of a packaged DSO. Finally, a 15 dB gain IF amplifier and proper mixing action in the monolithic mixer have been demonstrated. An additional iteration of the mixer, which was beyond the resources of this program, will however, be necessary for the final receiver front end. A functional block diagram of MMInc.'s "receiver on a chip" is shown in Figure 2-1.

Near the end of this program, sufficient MMICs were fabricated to deliver five of each type of MMIC (the LNA, the DSO, and the MXR/IF) to NASA Lewis Research Center for engineering data correlation. A photograph of the items delivered to NASA is shown in Figure 2-2. As previously mentioned, one of the DSOs was mounted in a housing with integral dielectric resonator. In addition, one of each of the other MMIC types was mounted on a custom carrier, and an RF test fixture designed to accommodate these carriers was also provided to NASA. The remaining four chips of each type were fully DC functional visually screened parts. Although to date only R&D quantities of the MMICs have been fabricated, initial yields indicate that low production costs will be readily attainable and that higher levels of monolithic integration might also prove cost effective.

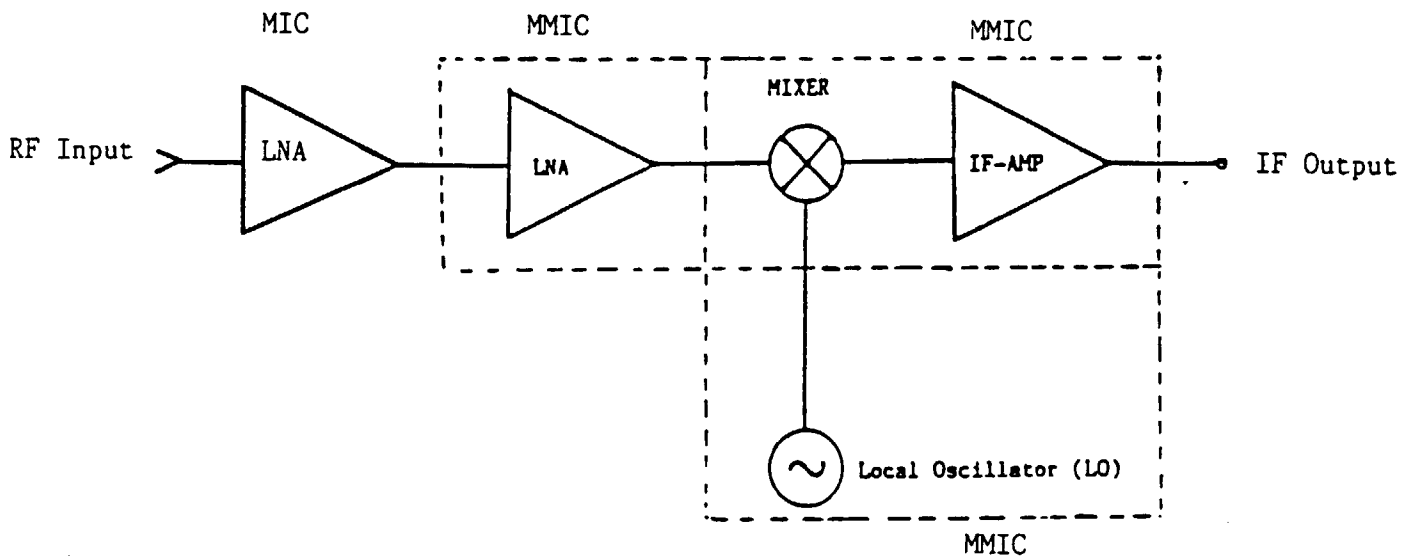


Figure 2-1) Functional Block Diagram of "Receiver-on-a-Chip"

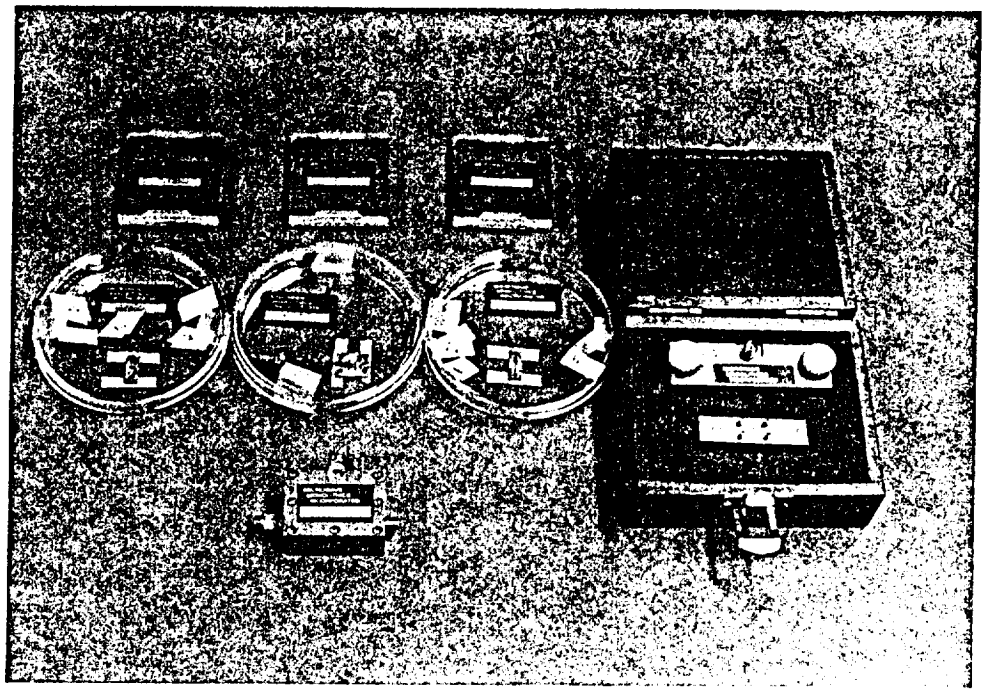
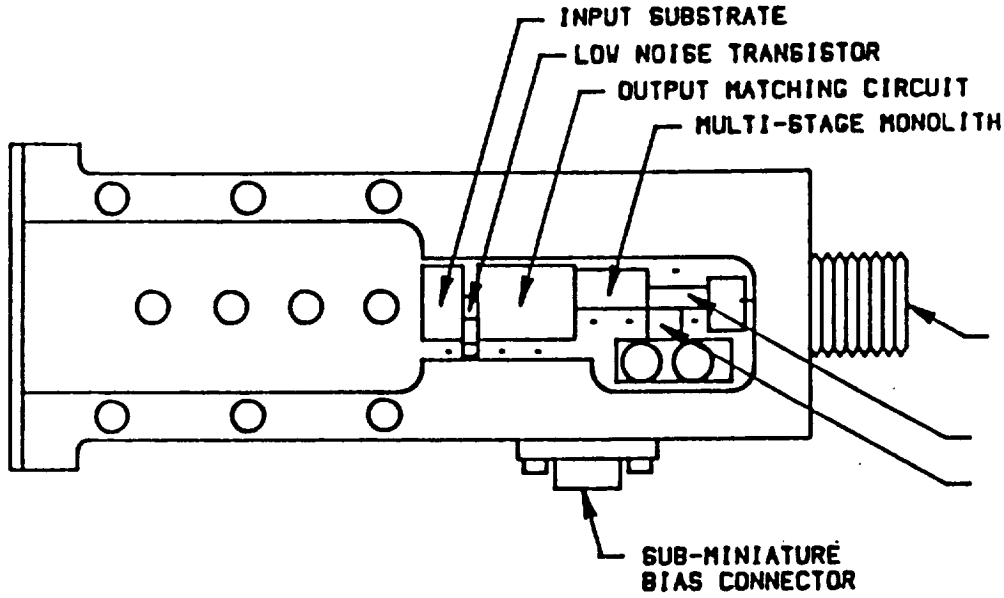
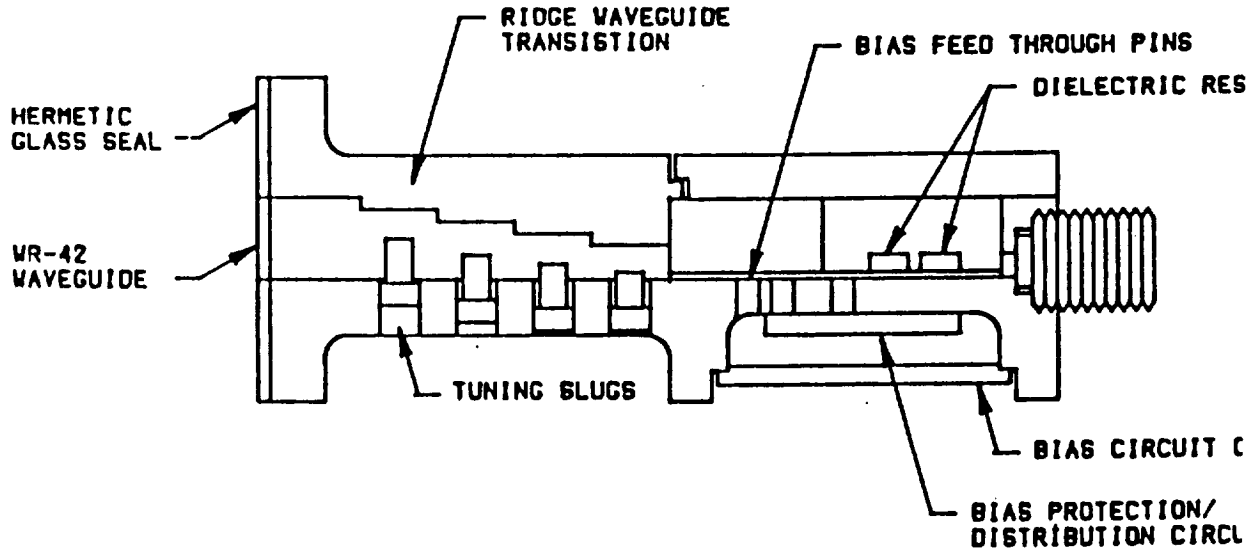


Figure 2-2) Photograph of Monolithic Receiver Front-End Components Delivered to NASA

Proof of concept for MMInc.'s low cost 20 GHz receiver front end design has thus been established. As originally envisioned by MMInc., a low risk phase III program consisting of a final MMIC design iteration followed by systems integration would therefore lead to completion of the hermetically sealed unit depicted in Figure 2-3. Completing development of this unit, or a similar one optimized to an alternate IF band selected by NASA, would help realize the full potential of NASA's thrust towards next generation 20/30 GHz communications satellite technology.



TOP VIEW - COVERS REMOVED



SIDE CENTER - SECTION VIEW

Figure 2-3) Integrated Waveguide Downconverter Utilizing MMICs

the right source and load impedance. To remedy this a small amount of shunt feedback in the form of an RLC circuit was placed between the gate and the drain of the FET. The feedback circuit was optimized to maximum out-of-band stability with minimum in-band noise figure degradation. The noise figure rose slightly at the low frequency while the stability factor, K, rose substantially especially at the low frequencies.

The LNA design approach was to use a two stage module to obtain simultaneous optimization of the noise figure, the gain flatness and the output reflection match. The first stage input circuit was designed to match the input admittance to the optimum source admittance (Y_{opt}) of the FET. The Y_{opt} admittance was calculated using the proprietary computer program MONO. The output of the first stage was initially optimized for maximum power gain. Two identical stages were then cascaded and all the circuit elements were re-optimized for minimum gain ripple, noise measure, and output reflection coefficient using a weighted error function. (Noise measure is the noise figure of an infinite number of cascaded amplifiers with the same gain and noise figure). The noise measure optimization thus prevents the optimization from minimizing the noise figure at the expense of gain. This is particularly necessary to account for the noise contribution of additional amplifier stages.

The optimized circuit diagram of the two-stage LNA circuit module is shown in Figure 3.1-1. The gain and noise figure responses of the cascaded four-stage LNA circuit are plotted in Figure 3.1-2, and the corresponding predicted input and output return losses are plotted in Figure 3.1-3. The predicted performance results of the LNA are summarized in Table 3.1-2. The LNA circuit is designed to fit on a 1.5 by 2.5 mm size chip. The two identical two-stage modules are internally connected at the mid-point of the chip, with provision to separate the two parts if necessary. The second module is topologically the mirror image of the first module along the center-line of the chip for maximum separation of critical elements such as through-substrate via-holes. A computer-generated pen-plot of the MMIC portion of the LNA is shown in Figure 3.1-4.

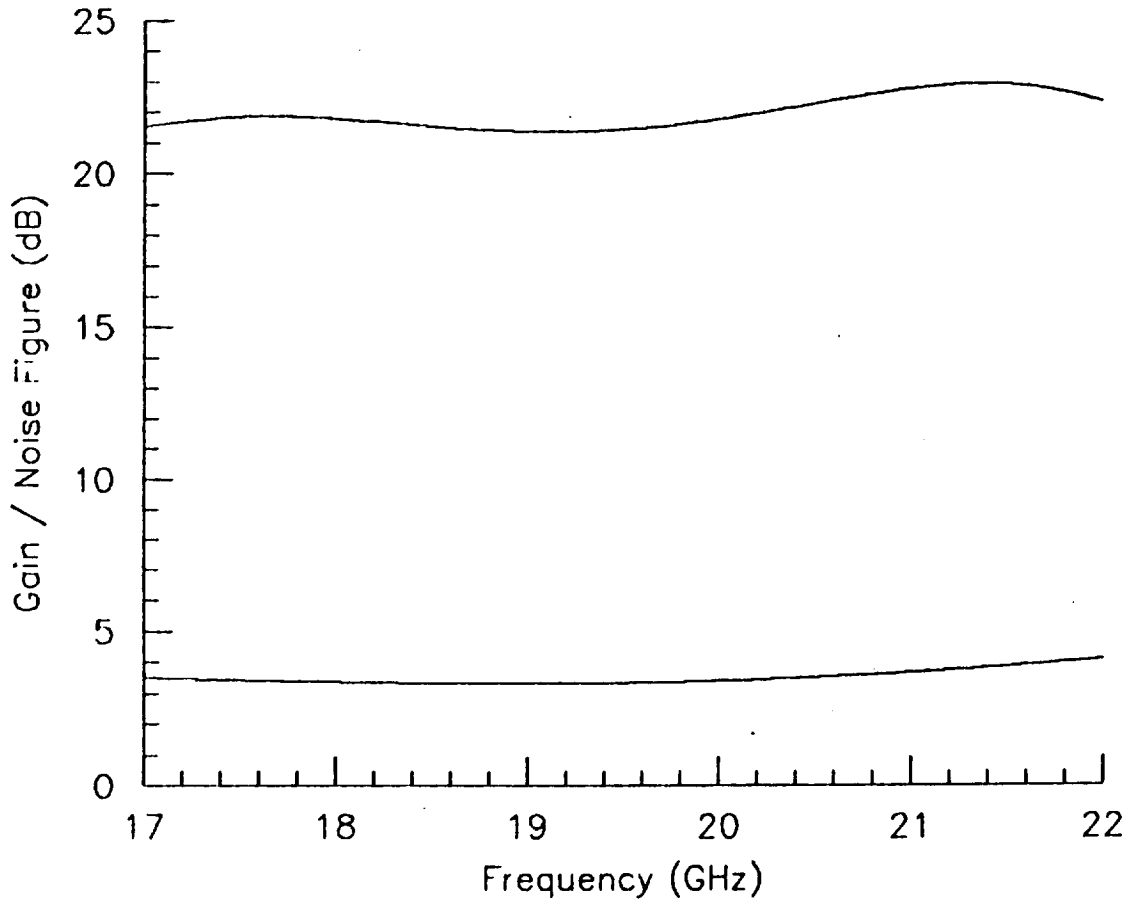


Figure 3.1-2) Predicted Gain and Noise Figure Response of MMIC LNA

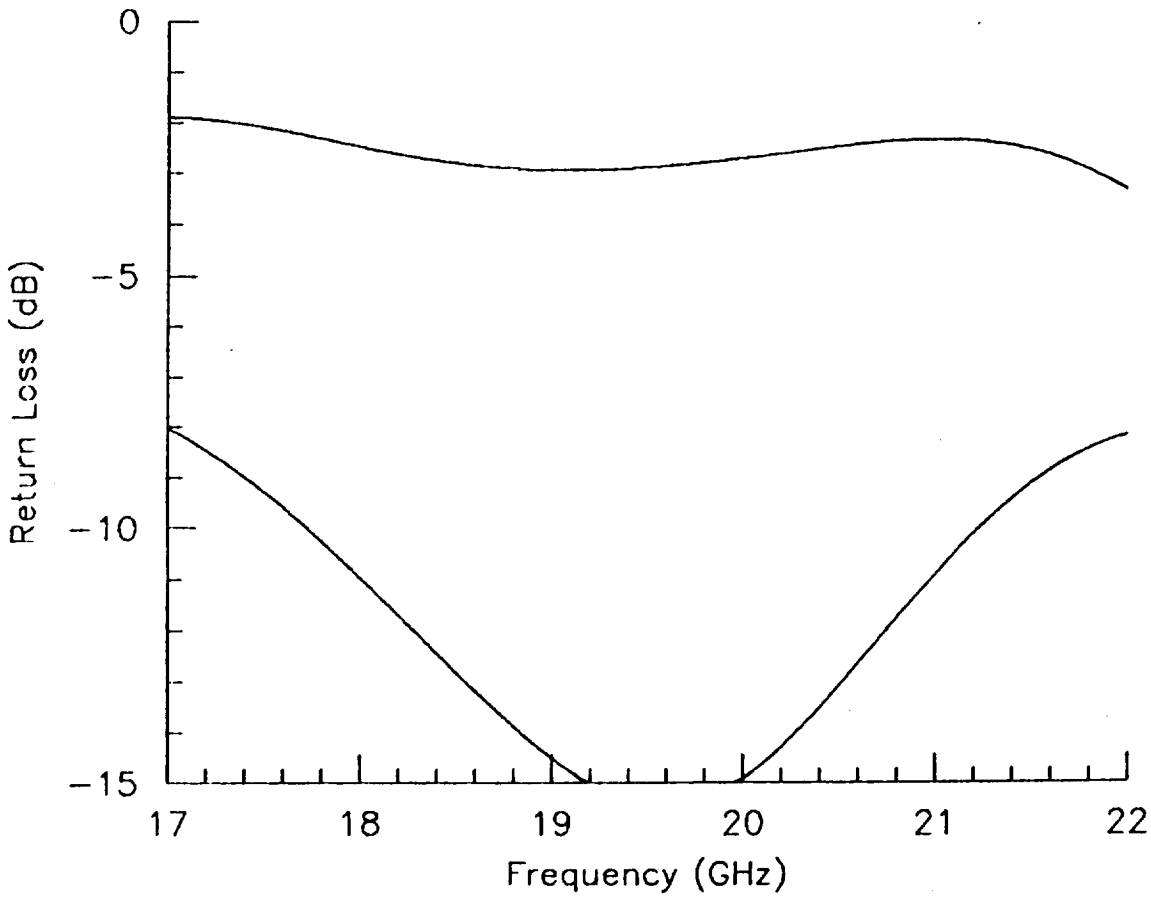


Figure 3.1-3) Predicted Input and Output Return Losses of MMIC LNA

Table 3.1-2 Predicted Performance of LNA

Frequency Range	17.7-20.2	GHz
Extended Range	17.0-21.2	GHz
Noise Figure	3.05	dB Max.
Noise Measure	3.06	db Max.
Minimum Gain	25.63	dB
Maximum Gain	26.34	dB
Gain Flatness	0.71	dB
Max. Gain Slope	0.001	dB/MHz
Output Return Loss	20	dB Min.
Reverse Isolation	50	dB
Phase Dev. from Linear	$\pm$2.0	Degrees
Min. Group Delay	0.21	nsec.
Max. Group Delay	0.30	nsec.
Chip Size	3.0	sq. mm
Prime Power	300-400	mWatt

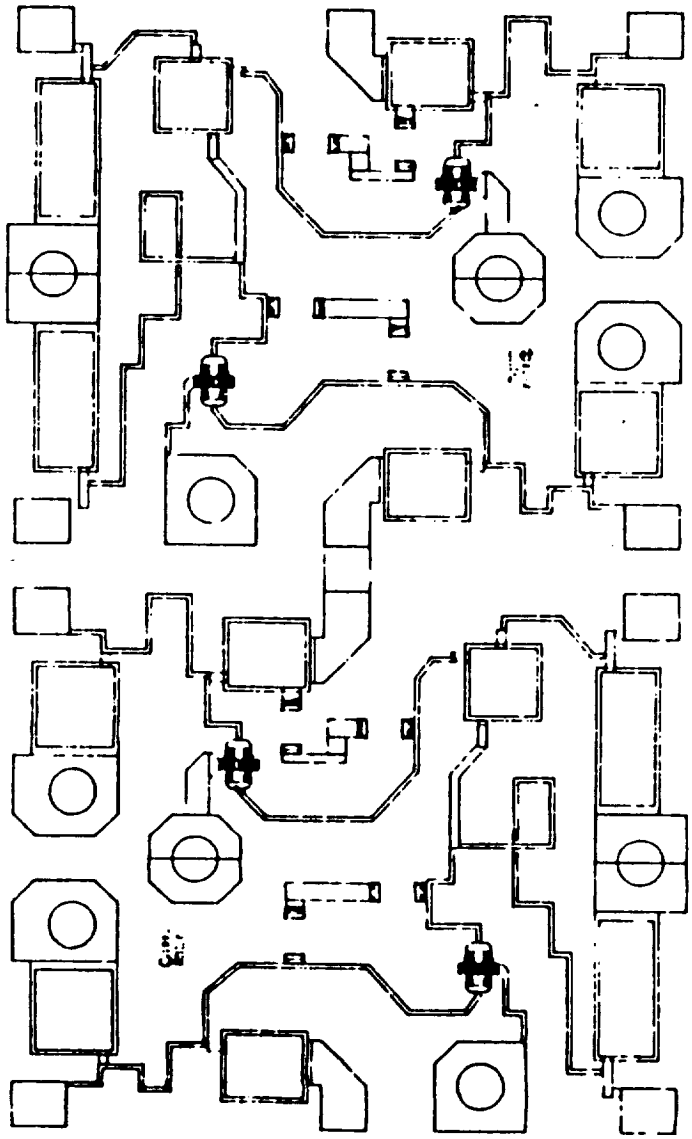


Figure 3.1-4) Computer-Generated Pen-Plot of the LNA MMIC Chip

3.2) LOCAL OSCILLATOR (LO)

The design of the monolithic local oscillator for the receiver front-end is described in this section. Several possible LO schemes were evaluated in program phase I, taking into consideration their performance, cost, and compatibility with monolithic integration, and the dielectrically stabilized FET oscillator was ultimately chosen. The final design consists of a monolithically integrated LO circuit with the exception of the dielectric resonator. The latter, due to its large size compared to the MMIC chip, is coupled to the MMIC resonator port via a microstrip transmission line inside the housing/package.

Having established at least a relative basis for evaluation, three basic LO approaches (with several different implementation options in each) were considered. These were a dielectrically stabilized FET oscillator approach, a diode oscillator approach (i.e., Gunns and IMPATTs), and multiplier chain approaches. A comparison chart summarizing the advantages and disadvantages of each configuration is presented in Table 3.2.1-1.

FET oscillators offer several advantages over two terminal IMPATT and Gunn oscillators. Output power is comparable to the Gunn oscillator but the efficiency is significantly better (10 percent compared to 1 percent for the Gunn). In addition, FET oscillators produce lower phase noise and improved stability compared to IMPATT oscillators. FET oscillators provide significantly improved reliability over diode oscillators since IMPATTs are sensitive to voltage breakdown and Gunns generate excessive heat. FETs also provide a wide variety of circuit configuration options which are not available with two terminal devices and are compatible with current GaAs monolithic implementation techniques. For example, several FET oscillators can be made on a single monolithic wafer. This is useful for power combining or selectively switching between different oscillators for multi-band coverage. It also permits a simplified low cost, planar circuit implementation. It was therefore determined in program phase I that a FET oscillator represents the best approach to the monolithic local oscillator requirement.

Three terminal FET oscillators can be classified as either reflection (negative resistance) or feedback oscillators. In the case of a reflection oscillator, the initial design of the oscillator includes utilization of either an unstable device or external (low Q) feedback to obtain negative resistance. A high-Q resonator is placed approximately one-half wavelength away from the FET on a terminated transmission line. Only at the resonant frequency does the load on the gate appear reactive; hence, oscillation occurs at that frequency due to the negative resistance of the FET. An example of this circuit is shown schematically in Figure 3.2.1-1.

Table 3.2.1-1) Trade Off Comparisons of LO Sources

Source Type	Advantages	Disadvantages
Multiplier Chains	Crystal Dependent Stability Matured Technology	High Cost/Excessive Circuitry High Phase Noise Spurious Signals Introduced Large Size Excessive Prime Power Reduced Reliability
Impatt Diode DSO's	Significant Cost Advantages Small Size	Reduced Stability Poor Phase Noise Poor Reliability
Gunn Diode DSO's	Moderate Cost Advantage Small Size Good Phase Noise	Reduced Stability Poor Power Efficiency Poor Reliability
FET DSO's	Significant Cost Advantage Small Size Consumes Low Prime Power Highest Reliability Monolithically Integratable	Reduced Stability Higher Phase Noise

Feedback oscillators can be divided into two classes: shunt and series type feedback oscillators. Examples of these two circuits are shown in Figures 3.2.1-2 and 3.2.1-3 respectively. In these circuits a resonator is placed in the feedback circuit of an amplifying FET. In a shunt feedback arrangement the resonator is placed between the output and input of the device (such as between the gate and source or gate and drain of the FET). In these cases the resonator impedance produces sufficient negative feedback only at the resonant frequency of the resonator. In the feedback configurations the resonator very strongly couples the input and output of the device. Therefore, the loaded Q of the circuit is quite low and the phase noise is degraded. Conversely, in the negative resistance oscillator the resonator is only weakly coupled, thus producing a higher loaded Q circuit with better phase noise performance.

The stability, phase noise and resonant frequency of the oscillator is determined largely by the characteristics of the resonator. Two types of resonators may be considered for microwave oscillators: dielectric resonators and metal-wall cavities. In both cases the resonant frequency is proportional to the diameter of the cylindrical resonator. Metal-wall cavities are commonly used in waveguides for use as frequency wavemeters. Without dielectrics the Q is inversely proportional to the conductor losses on the walls of the cavity. Unloaded Q in excess of 10,000 are theoretically possible at 10 GHz with copper conductors. The fields are electrically coupled to the circuit with slots in the metal-wall. Conversely, dielectric resonators are magnetically coupled to the circuit. The unloaded Q of these resonators are determined (inversely) by the loss tangent of the dielectric material. The unloaded Qs are somewhat lower than the metal-wall cavity even with the best material available. However, the dielectric resonator offers a significant size advantage proportional to its relative dielectric constant. Furthermore, dielectrics can be made with adjustable temperature coefficients (both sign and magnitude) to achieve temperature stability in the oscillator by compensating for changes in the housing temperature.

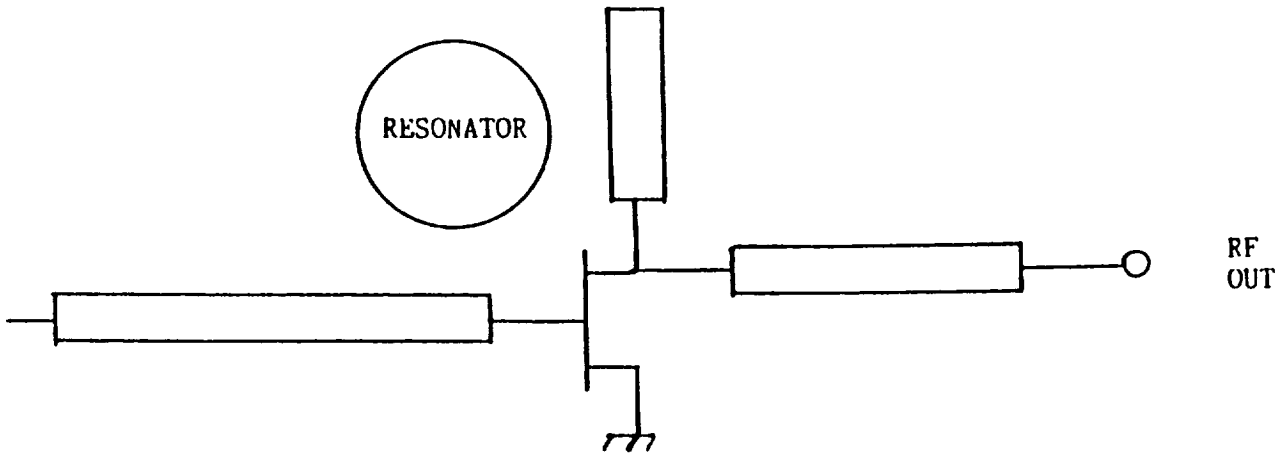


Figure 3.2.1-2) Typical Shunt Feedback Oscillator Configuration

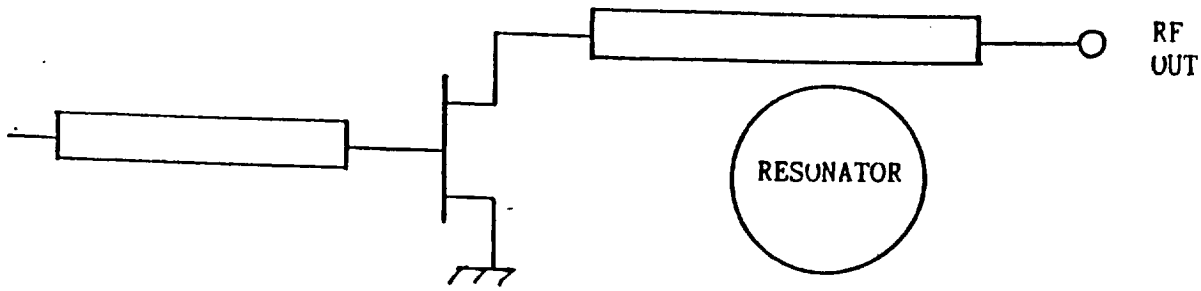


Figure 3.2.1-3) Typical Series Feedback Oscillator Configuration

Multiple dielectric stabilized oscillators can be implemented in a receiver using a couple of configuration methods as shown in Figures 3.2.1-4 and 3.2.1-5. In the first figure a FET switch is used to select the mixer local oscillator (LO) source from two or more DSOs. In the second figure, the switch is used to select only the dielectric resonator which determines the LO frequency from a common oscillator. This latter approach appears preferable on the surface since it uses less parts and would therefore be more reliable. However, this is not necessarily so. If a system were configured using overlapping intermediate frequency (IF) bands and the DSO frequencies were selected to utilize this feature, then the switched DSO approach would actually be more reliable since it has redundancy in the oscillator. One problem with the second approach was determined during the design of the LO. The frequency of oscillation is somewhat sensitive to the transmission line length between the dielectric resonator and the input to the gate of the FET. Since the resonators must be magnetically isolated from each other, the positions of the resonators in the housing place severe limitations on the control of those line lengths. Another problem with that approach is that the FET, switch which is situated between the resonator and the FET reduces the effective overall Q of the circuit due to the transmission loss associated with the switch.

Although it is theoretically possible to switch between resonators as shown in Figure 3.2.1-4, the exacting phase relationships (lengths of the coupling 50 ohm lines) required for each resonator combined with the losses likely to be encountered in the switches, makes the alternative approach shown in Figure 3.2.1-5 more attractive. Provided the MMIC portions of each oscillator are identical, as is the case in the design presented above, and the unused oscillators are DC switched off to avoid spurious outputs and reduce power consumption, the final costs are not expected to be significantly increased. Indeed, the added tuning time, and cost, required for the circuit shown Figure 3.2.1-4 may make the approach shown in Figure 3.2.1-5 the lowest cost.

Considering the case of two bands, a resonant single pole double throw switch based on two FETs is shown in Figure 3.2.1-6. Here, the

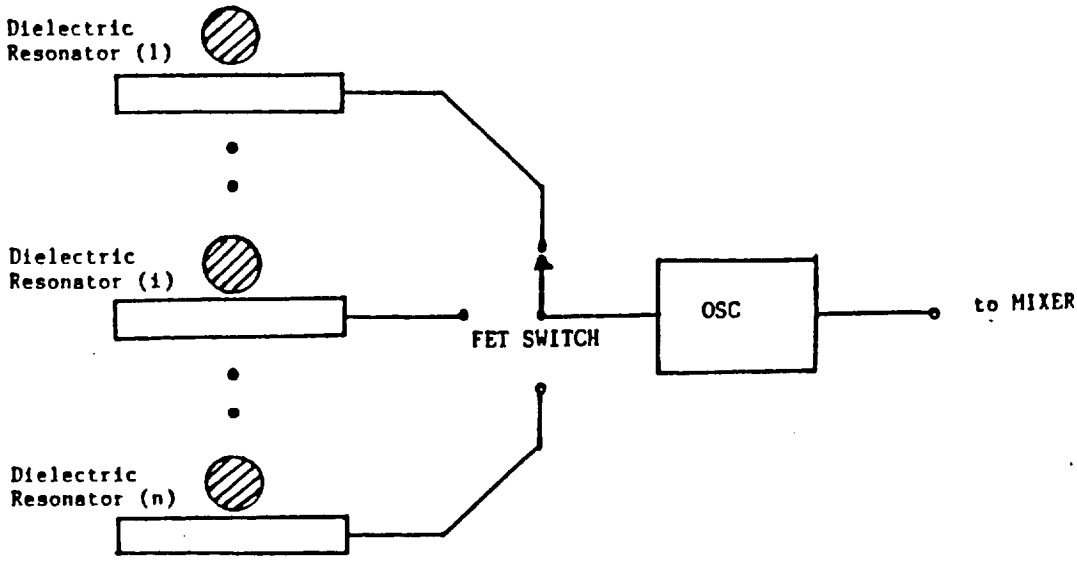


Figure 3.2.1-4) Band Switching via Switched Selected Resonators

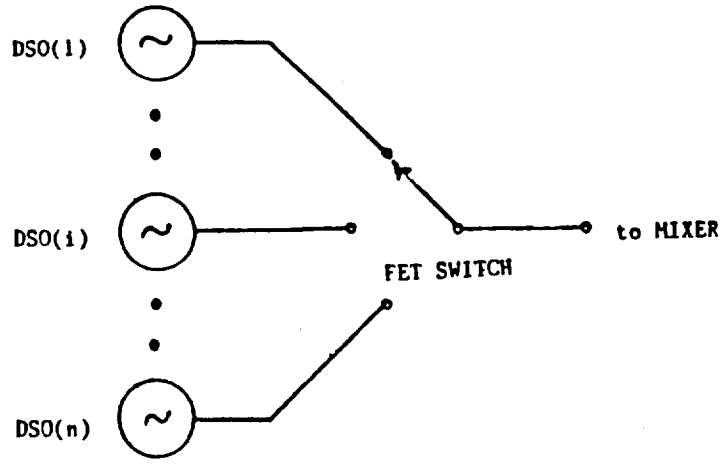


Figure 3.2.1-5) Band Switching via Switched Oscillator

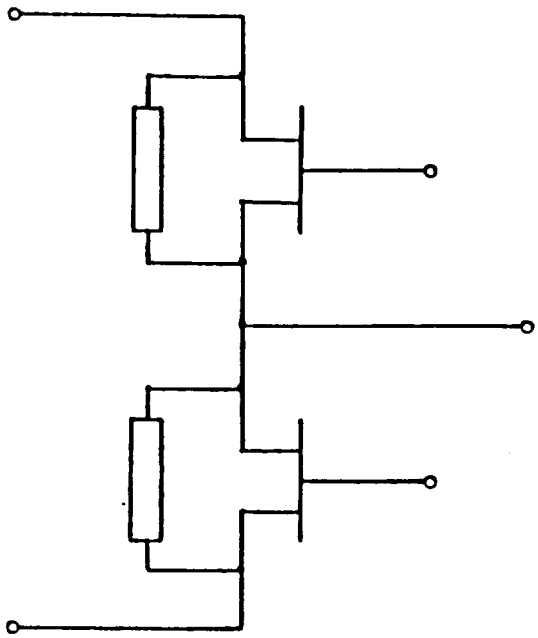


Figure 3.2.1-6) SPDT Passive FET Switching Circuit

obtain loop gain greater than unity, and the loaded Q is therefore high. Negative resistance oscillators, where the resonator and output are coupled to a separate ports, offer the potential for reduced phase noise and will be pursued here. A side benefit of this approach is that only one coupling line is required, (also true for the series feedback design approach) therefore only two RF bonding pads are required for the MMIC chip - a resonator coupling and an RF output port.

Although there are many wideband feedback network networks which will provide negative resistance, the circuit selected should also provide simple bias insertion and a minimum of crossovers for monolithic implementation. Figure 3.2.2-1 shows the circuit selected for the current application, including the integrated buffer amplifier. All bias voltages are supplied through tuning elements and there are no crossovers, therefore consumption of valuable GaAs real estate is minimized. Internal FET capacitances, combined with the series feedback generated by the source transmission line, provide a broadband negative resistance at both the gate and drain. The dielectric resonator coupled to the 50 ohm gate line reflects sufficient power to maintain oscillation, while the coupling coefficient is adjusted to maximize loaded Q and minimize phase noise. Length of the coupling transmission line is selected to provide positive feedback at the resonant frequency of the dielectric puck. The 50 ohm resistor beyond the resonator minimizes reflections out of band and eliminates spurious oscillations. Finally, the output matching network on the drain electrode of the 300 micron FET couples power from the oscillator to the buffer amplifier.

Design of the oscillator is initiated with the small signal S - Parameters of the FET, shown in Table 3.2.2-1. Although this FET is conditionally unstable over the 13 to 15 GHz band, additional series feedback is provided to insure strong oscillations. With this feedback, the output matching network, and the input delay line up to the resonator, the small signal S - Parameters are transformed as shown in Table 3.2.2-2. The placement of the resonator was set for 14 GHz in this calculation, which will be used in all of the following performance

estimates. Similar operation is achieved over the band by altering the resonant frequency and positioning of the dielectric resonator. No changes are required on the MMIC portion of the oscillator, shown inside the dotted lines in Figure 3.2.2-1.

For an estimate of the output power, a proprietary large signal analysis program named MMIC-SPICE was used to analyze the oscillator. Here, the simulation was run sufficiently long for the "turn on" transients to die out, resulting in a steady state output voltage waveform across the 50 ohm load resistor. The peak to peak output voltage was calculated to be 1.7 volts, therefore the RMS output power is 8.5 dBm.

Phase noise simulation is almost impossible by this technique due to the extremely long computer run times required to evaluate the close-in noise while stepping at a small fraction of an RF cycle. Small steps are necessary for numerical stability, while several cycles of the noise frequency must be analyzed to reach steady state. In addition, accurate noise models of the FET and coupling mechanisms are not available, making meaningful estimates elusive. Under the circumstances, it is advisable to perform actual phase noise measurements on a dielectrically stabilized monolithic oscillator.

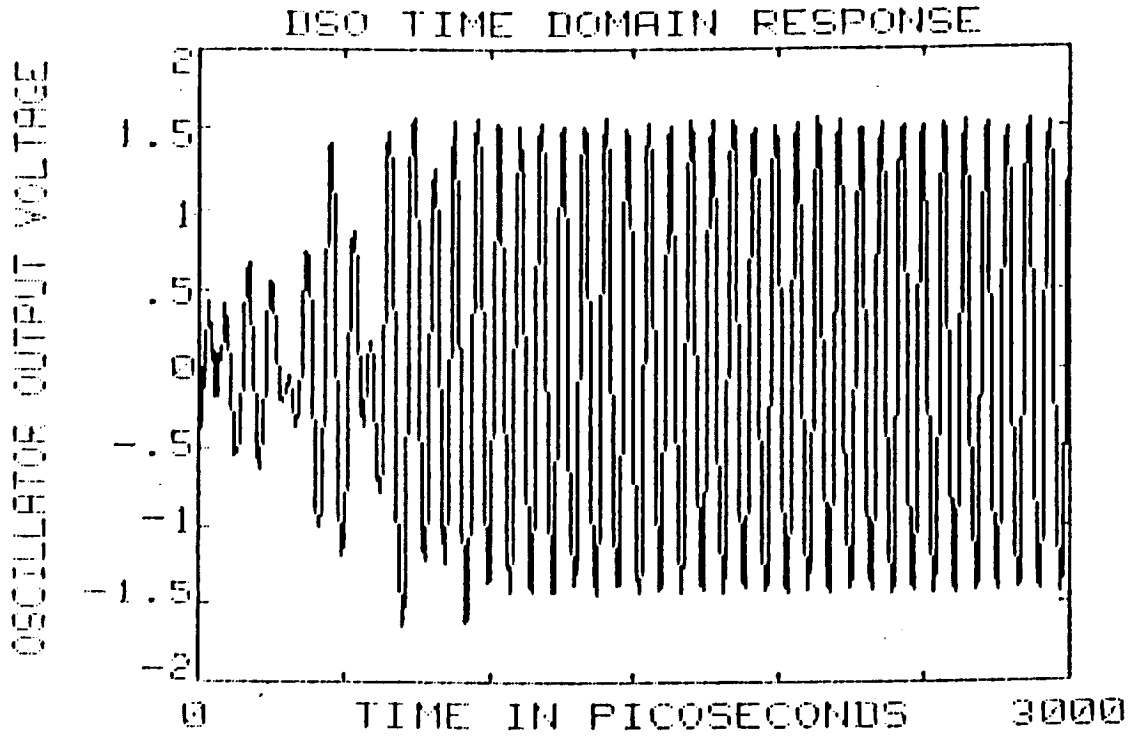
Buffer amplifier design is straightforward compared to both the low noise amplifier and the local oscillator. The only requirements are good reverse isolation for minimizing load pulling effects, which is automatically obtained by the FET amplifier, an input impedance compatible with the oscillator, moderate gain, sufficient output power capability. The single stage source follower amplifier shown on the right side of Figure 3.2.2-1 meets these needs. Its small signal scattering parameters are shown in Table 3.2.2-3. As in the oscillator design, all bias feeds and DC blocking capacitors are part of the matching network to minimize chip size. Note that it is important to integrate both the oscillator and buffer on the same chip to avoid phase variations between them which could alter output power or even quench oscillations. The output waveform of a large signal MMIC-SPICE analysis

Table 3.2.2-3 S - Parameters of the Buffer Amplifier

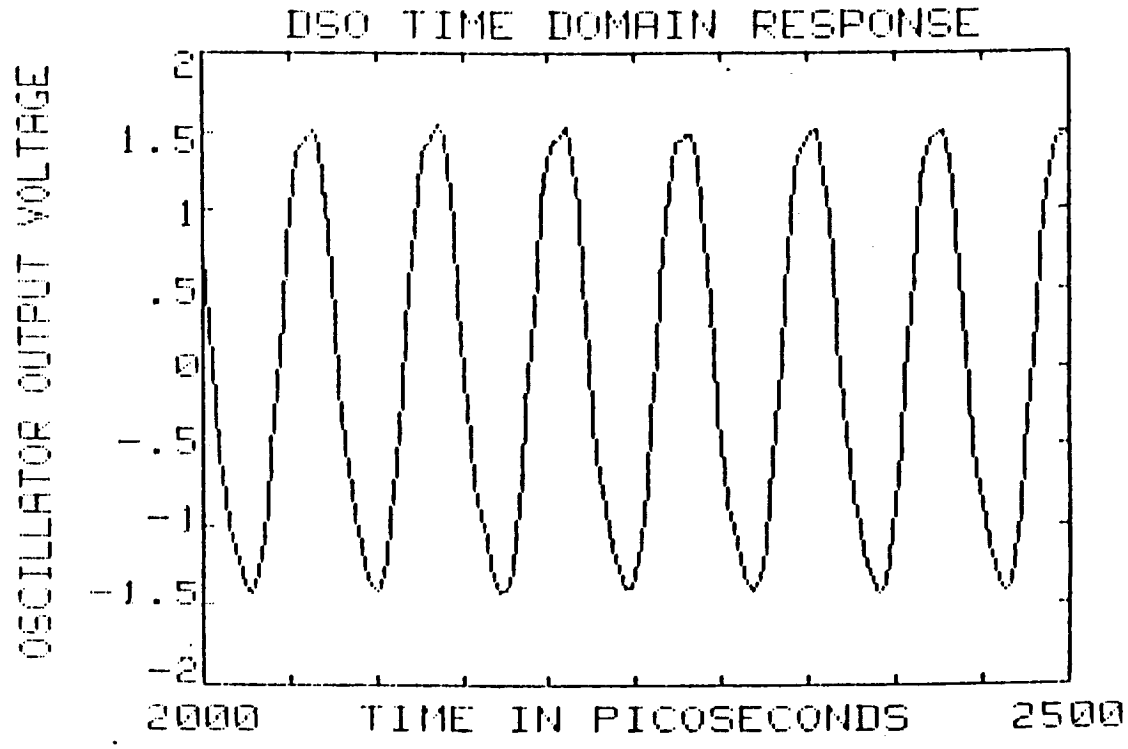
F(GHz)	S11		S21		S12		S22	S21(dB)
13.000	0.33<	9.4	0.86<	29.0	0.47<	92.	0.18<-154.9	-1.32
13.500	0.42<	3.5	0.82<	22.3	0.46<	84.	0.22<-142.2	-1.69
14.000	0.49<	-2.1	0.79<	16.5	0.46<	77.	0.26<-135.7	-2.08
14.500	0.55<	-7.3	0.75<	11.5	0.45<	71.	0.30<-132.7	-2.47
15.000	0.60<	-11.9	0.72<	7.2	0.44<	66.	0.33<-131.4	-2.85

of the combination oscillator/buffer amplifier is shown in Figure 3.2.2-2. Figure 3.2.2-2a shows the waveform from start-up to steady state, while Figure 3.2.2-2b is an expanded view of the steady state oscillation. Predicted output power is 13.5 dBm at the operating frequency of 14 GHz, well above the requirements of the mixer.

The monolithic LO circuit is just 1.0 by 1.5 mm. A computer-generated pen-plot of this compact MMIC LO layout is shown in Figure 3.2.2-3.



a) Start-up Through Steady-State



b) Expanded Steady-State Output Waveform

3.2.2-2) Output Waveform of the DSO/Buffer Amplifier Circuit

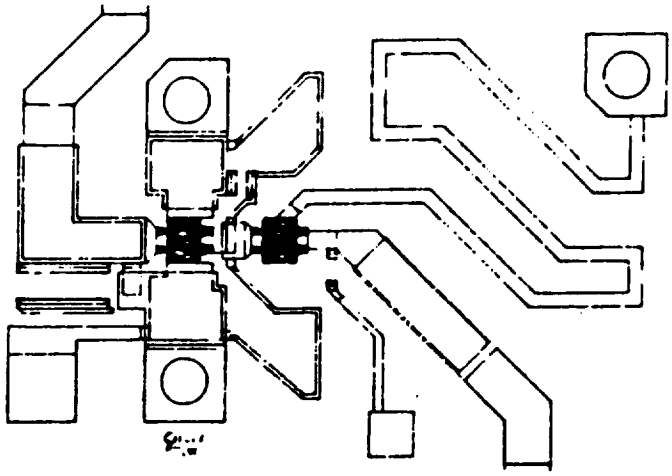


Figure 3.2.2-3) Computer-Generated Pen-Plot of the LO Chip

3.3) MIXER / IF AMPLIFIER (MXR/IFA)

Ideally the IF amplifier can be placed on the same monolithic GaAs chip as the mixer to facilitate matching between the two components and reduce complexity of the receiver front end. On chip matching eliminates the need to match each component to 50 ohms, thereby simplifying the design and construction of both. Since the mixer and the IFA will be physically small, cost increases due to reduced yield of the compound component are not expected to be significant. Cost savings due to reduced assembly and test requirements are, however, expected to be beneficial. For the purpose of individual testability, the mixer and the IFA circuits are nevertheless matched to 50 ohms, with an interconnection transmission line utilized to form a single MMIC chip.

A monolithic mixer has several advantages over conventional hybrid mixers. By using either a common drain or common source FET on the mixer RF and LO input points to drive the Schottky barrier mixer diodes, significant LO and RF isolation is obtained since the FETs are inherently nonreciprocal. Configuration choice depends upon the desired impedance level. Common drain configurations provide a higher input impedance than does common source.

By using a FET driven mixer, large sized hybrids and couplers are avoided, hence a balanced mixer can be made on a single "chip" less than one square millimeter in size. The small size provides another advantage in that the RF and LO matching can be done very close to mixer diode while using the input FETs as impedance/isolation transformers. This broadbands the mixer circuit response.

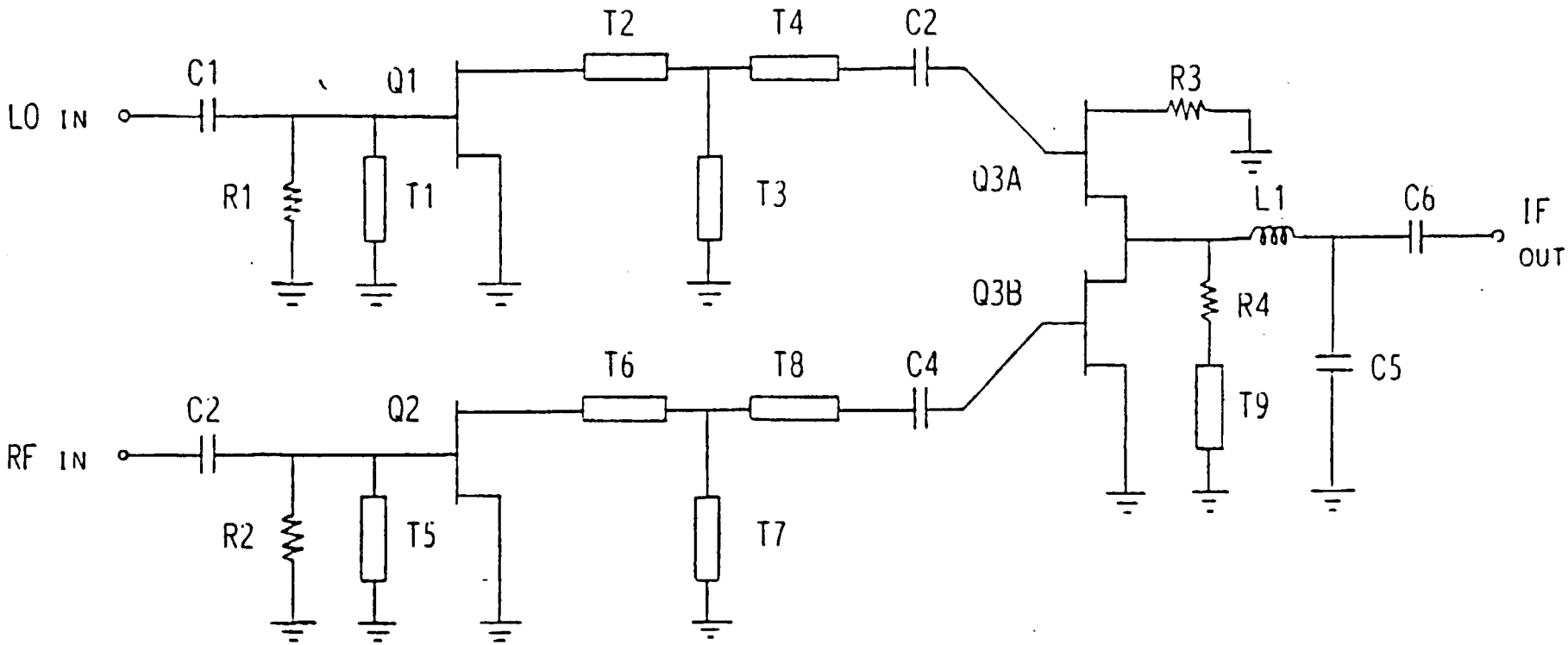
Another advantage of the monolithic mixer is that the IF amplifier can be integrated on the same circuit of the mixer. The advantage of this integration is that the IF amplifier input impedance can be matched directly to the mixer output impedance without having to match both circuits to an arbitrary 50 ohm intermediate impedance. The significance of this feature is that the combination response has a lower noise figure, less gain ripple, and a broader bandwidth. In

addition, circuit size is reduced. Furthermore, test time is minimized since both circuits can be evaluated as one unit.

The mixer can be configured either as a single ended mixer driven by an FET on the RF and LO leads or as a balanced mixer using semi-lumped element hybrids. The single ended mixer is less complicated than the balanced mixer and can be realized in a smaller size configuration since it does not require hybrid circuits. The balanced mixer has higher level intercept points and consequently the spurious mixing harmonics will be somewhat lower than with the single ended approach.

Considering the fairly high gain (25dB) of the monolithic LNA chip, a relatively simple mixer design is appropriate. The schematic diagram of the mixer circuit is shown in Figure 3.3-1. The design consists of common-source FET amplifier stages for the RF and LO ports respectively driving a dual gate FET mixing element. A low-pass filter connects the output of the mixing stage to the IF port. The configuration of the driver stages are similar; the frequency range can be adjusted for a particular application by changing only one mask level. The conversion loss of the FET driven mixer is nominally 0 dB. The mixer chip is designed to fit into a 1.5 by 1.5 mm size chip. A computer-generated pen-plot of the monolithic mixer chip is shown in Figure 3.3-2.

With the design of the RF components as described in the previous sections, the requirements of the IF amplifier are not severe. The 5 dB noise figure requirement is ample justification to describe the IF amplifier as a non-critical component. The margin between this and the FET device minimum noise figure of typically 1 dB allows the design to be based on low cost fabrication utilizing small chip size for further component cost reductions. For example, the use of inductive tuning must be minimized since the size of these elements at the IF frequencies is many times the size of the FET amplifying devices. However, the frequency is high enough that they can not be totally eliminated if a reasonable noise figure is desired. Noise figures much higher 5 dB would however be detrimental to overall receiver performance.



MIXER NOISE FIGURE < 8 dB.

MIXER GAIN = 0 dB

Figure 3.3-1) Schematic of the Monolithic FET MIXER Circuit

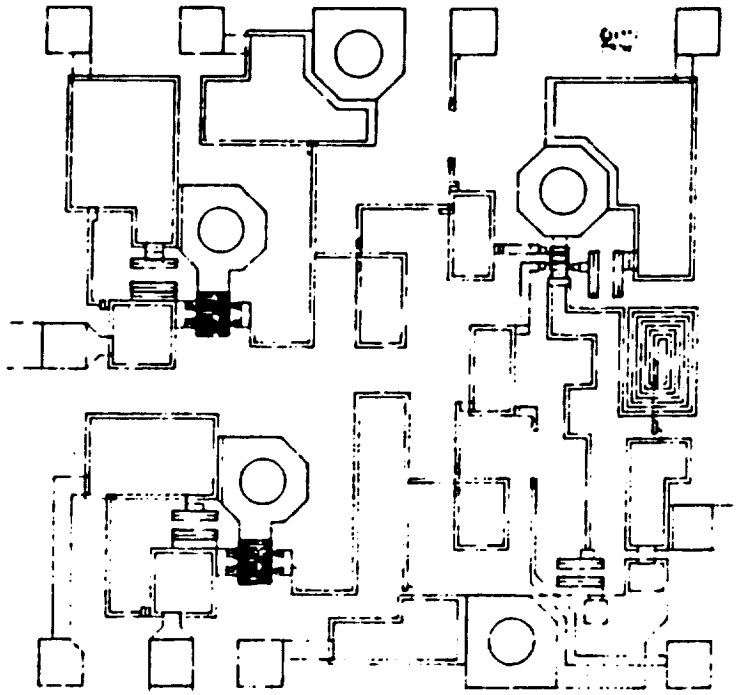


Figure 3.3-2) Computer-Generated Pen-Plot of the MIXER Chip

With these guidelines, the schematic diagram of an IF amplifier for the 20 GHz low cost receiver front-end is shown in Figure 3.3-3. A common-gate configuration is used for the first stage to provide a good input match. A common-source second stage provides good gain. Good output match is provided by a common-drain (source-follower) third stage. DC power is supplied through active loads on all three stages resulting in substantial savings in GaAs real estate. DC source return for the first stage is provided through a spiral inductor. The gate bias for the second stage is likewise supplied through another spiral inductor which also provides some tuning for gain. The gate of the third stage is nominally self-biased with provision for external adjustment if needed.

The IF amplifier circuit shown in Figure 3.3-3 has a predicted gain above 16 dB, and a predicted noise figure well below 4 dB at room temperature. The predicted gain and noise figure performance of the IF amplifier over frequency is shown in Figure 3.3-4, and the input/output return loss is shown in Figure 3.3-5. This compact circuit is only 1.5 by 0.9 mm. A computer generated pen-plot of the monolithic IF amplifier circuit is shown in Figure 3.3-6. The mixer and IFA circuits shown in Figures 3.3-2 and 3.3-6 form a single 1.5 by 2.5 mm size chip.

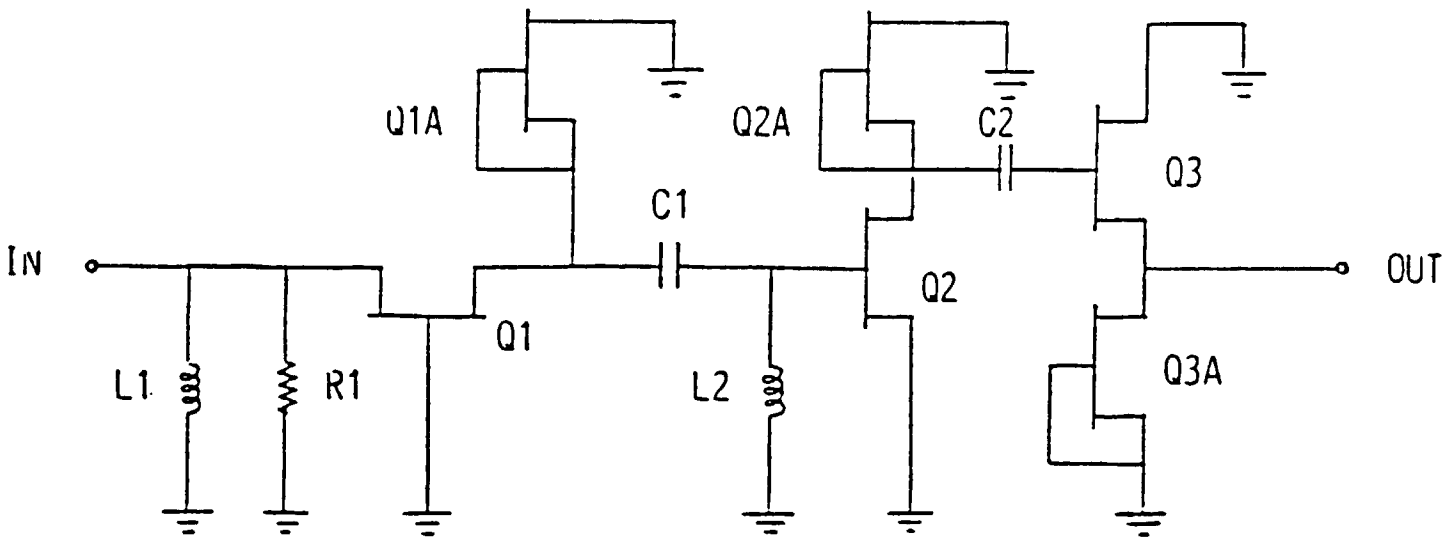


Figure 3.3-3) Schematic Diagram of the Monolithic IF Amplifier Circuit

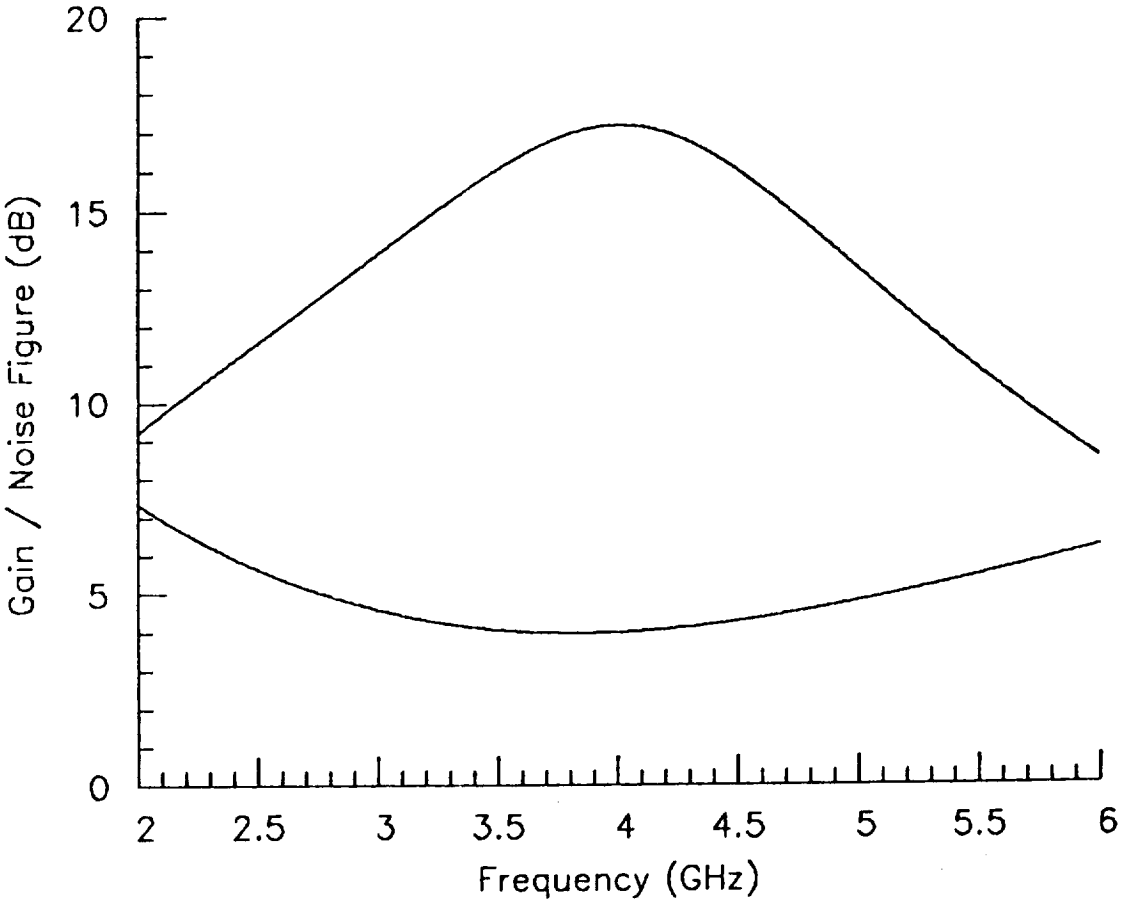


Figure 3.3-4) Predicted Gain and Noise Figure Response of MMIC IFA

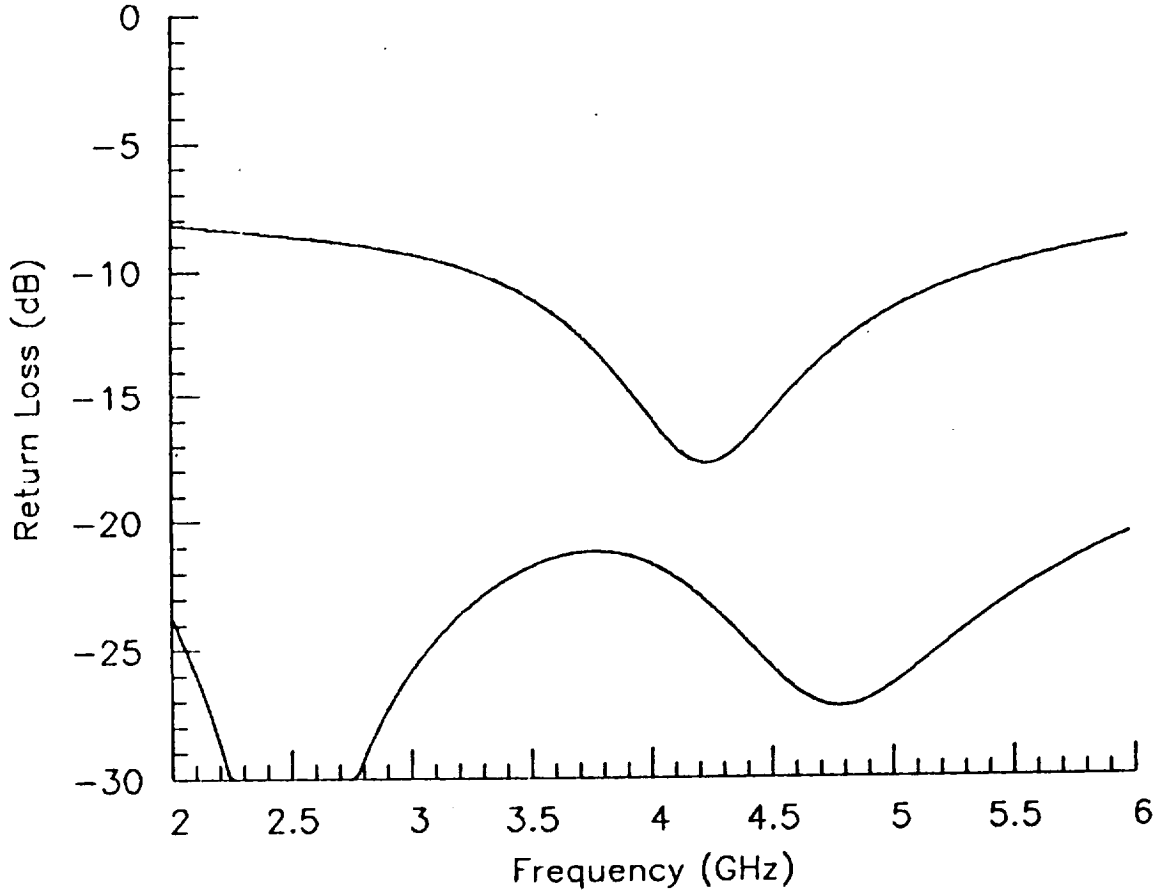


Figure 3.3-5) Predicted Input and Output Return Losses of MMIC IFA

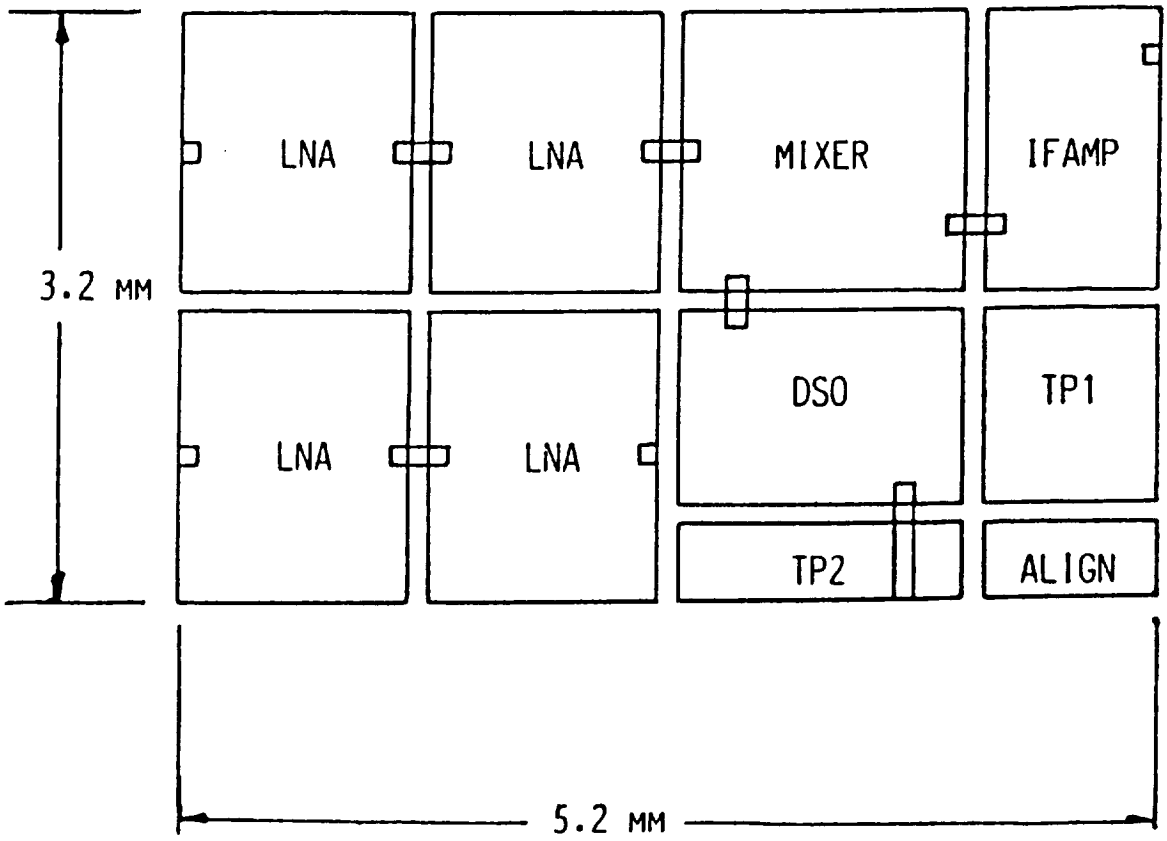


Figure 3.4-1) Mask Layout of 20 GHz Monolithic Receiver Front-End

3.5) MIC LNA FIRST-STAGE / RECEIVER-MMIC INTERFACE

The effects of expected parameter variations, both from wafer to wafer as well as across the wafer, on the performance of the monolithic receiver front-end must be considered to complete the circuit design. Performance acceptance criteria should be confined to realistic ranges; "yield-to-specification" may otherwise suffer. The relevant parameters are the system noise figure, which is primarily determined by the noise figure of the first stage of the LNA, and the overall gain. Since noise match is very sensitive to parameter variations and the circuit noise figure is already close to the device minimum noise figure, a range of noise performance should be expected. On the other hand, the small-signal gain is expected to exhibit a tighter distribution with a large percentage of circuits satisfying the minimum requirement.

MMInc.'s design approach therefore utilizes an MIC first-stage LNA in the implementation of the 20 GHz receiver front-end subsystem, as shown in Figure 3.5-1. This configuration has been selected to increase the overall yield and lower ultimate production costs. In this scheme, the single-stage MIC LNA provides moderate gain (about 6 dB) and low noise figure (well below 3 dB). The MMIC LNA still provides substantial gain; the noise figure requirement is however considerably relaxed since the overall noise figure is now primarily set by the MIC first-stage. The extra cost of assembling and tuning the MIC component may be offset by the savings from increased yield-to-specification of the MMIC chip. The individually tuned first-stage may actually consist of a MMIC chip with complete matching circuitry on the output side and uncommitted gate connection on the input side. This will result in some savings in labor associated with MIC assembly and tuning. This "first-stage" may even be combined with the MMIC LNA into a single RF chip. Furthermore, the input matching circuitry for the individually tuned first-stage need not be restricted to MIC implementation. It is in fact advantageous at the RF frequency (20 GHz) to put at least part of the circuitry in the waveguide section which in turn interface to the antenna. Lower loss is possible with this scheme. More convenient tuning is possible, which may be accomplished by automatic test equipment setups. The waveguide

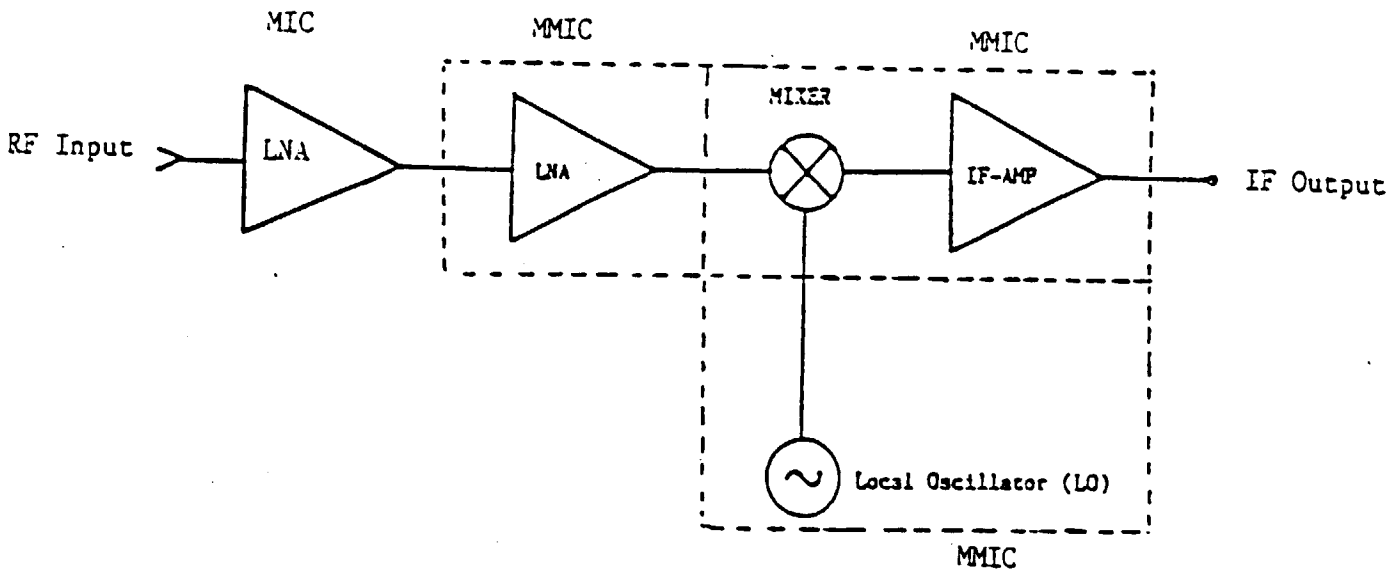
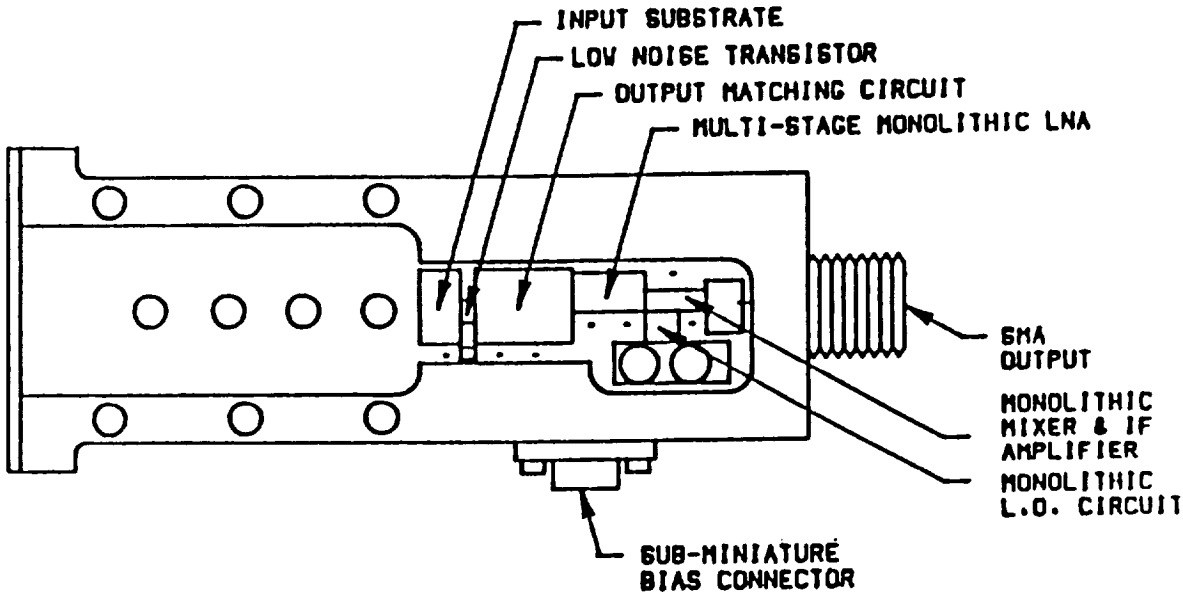
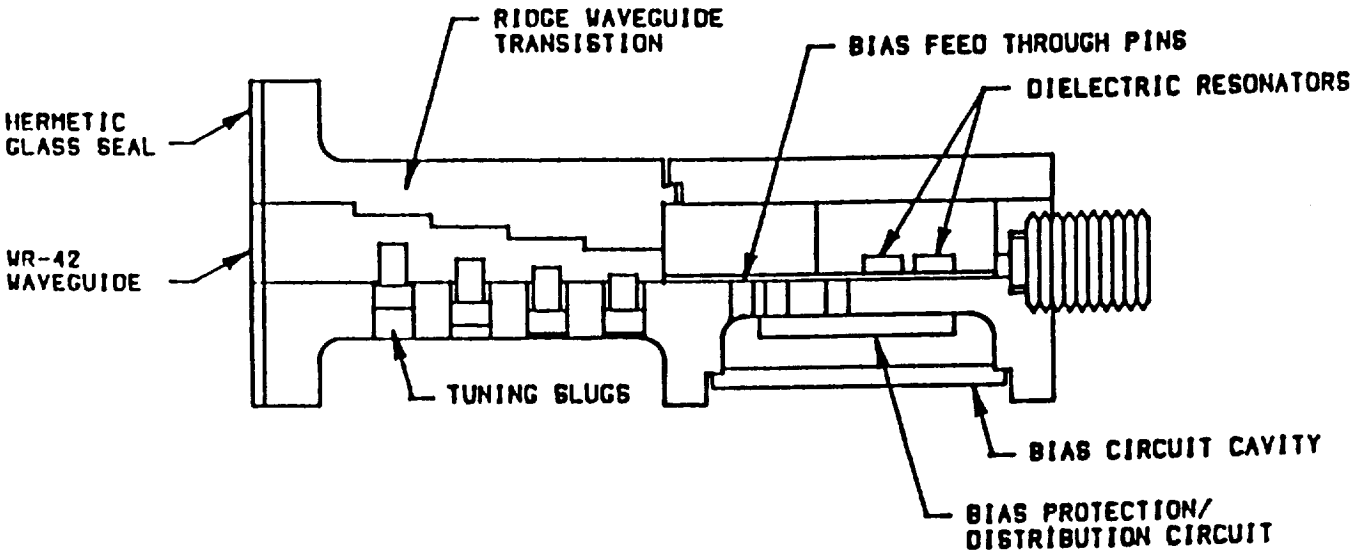


Figure 3.5-1) Block Diagram of Downconverter with MIC LNA Stage and MMICs



TOP VIEW - COVERS REMOVED



SIDE CENTER - SECTION VIEW

Figure 3.5-2) Waveguide Downconverter Package Utilizing MMICs

4.1) FET Device Design

Based on past experience and published data on FET noise figure,[2,3,4,5] a gate length of 0.5 microns or less is required to meet the present device goals in noise figure and gain. In order for the FET to operate properly, i.e. good control of drain current by gate voltage (high transconductance) and low modulation of drain current by drain voltage (low drain conductance), the minimum aspect ratio of gate length to channel thickness is about 3. This translates to a maximum channel thickness of 0.15 microns. The materials technology must then be capable to repeatably produce such thin active layers with sharp interface with the substrate.

Several other aspects of FET device design must also be addressed for high gain and low noise besides short gate length. In a normally processed gate the cross-section would decrease with the gate length. This is in fact quite severe since the thickness of metalization must also be decreased due to use of a thinner resist layer for pattern definition. This would lead to loss at the FET input and contribute to the device noise figure. Hence the cross-section of the gate must be kept large while the "footprint" of the gate, which defines the electrical gate length, is reduced. Another contribution to the device noise figure is the source resistance. This consists of two parts: the ohmic contact resistance and the source-to-gate series resistance. Both of these are affected by the sheet resistance of the semiconductor material (outside the intrinsic FET region). The source resistance can be reduced by heavily doping the source and source-to-gate regions. The active channel must of course remain unaffected.

4.2) Flash Annealing

Ion implantation is a proven materials technology for GaAs FET and MMIC fabrication. Its advantages include simplicity of process, high uniformity and repeatability, and potential high throughput in volume production. The very thin active layer required by the present FETs is usually difficult to reproducibly prepare by other methods such as VPE (vapor phase epitaxy). The doping profile of ion implanted active layers, on the other hand, is determined by scattering at the atomic level, and is inherently predictable. Implantation into state-of-the-art bulk grown semi-insulating GaAs and high purity buffer layers has demonstrated excellent control of activation. This is hence a viable materials technology for accomplishing the program goals.

A severe limitation associated with conventional ion implantation technology is the requirement of annealing at temperatures of 850^{o}C for periods of 30 minutes. For example, the diffusion length of Si in GaAs due to this annealing cycle is about 0.06 micron. This would certainly degrade the implant layer for the required devices. A method developed at MMInc., the Flash Annealing technique, reduces the dwell time at high temperature drastically, from typically 30 minutes to less than 10 seconds. A typical temperature versus time profile of a flash annealing cycle is shown in Figure 4.2-1. A peak temperature of nearly 1000^{o}C can be reached in about 5 seconds. Good activation has been obtained at peak temperatures as low as 800^{o}C.* Diffusion of impurities has been shown to be minimal. The quality of the annealed material is excellent as indicated by the high mobility. Low sheet resistivity n^{+} layers have also been obtained using this method. Ti-W/Au Schottky barrier gates on n-GaAs which have been shown to exhibit insignificant degradation in diode characteristics at processing temperatures up to 900^{o}C are also compatible with the Flash Annealing process.

* (Unpublished data by Microwave Monolithics Incorporated under contract with the Department of the Navy, Contract no. N00014-82-C-0605.)

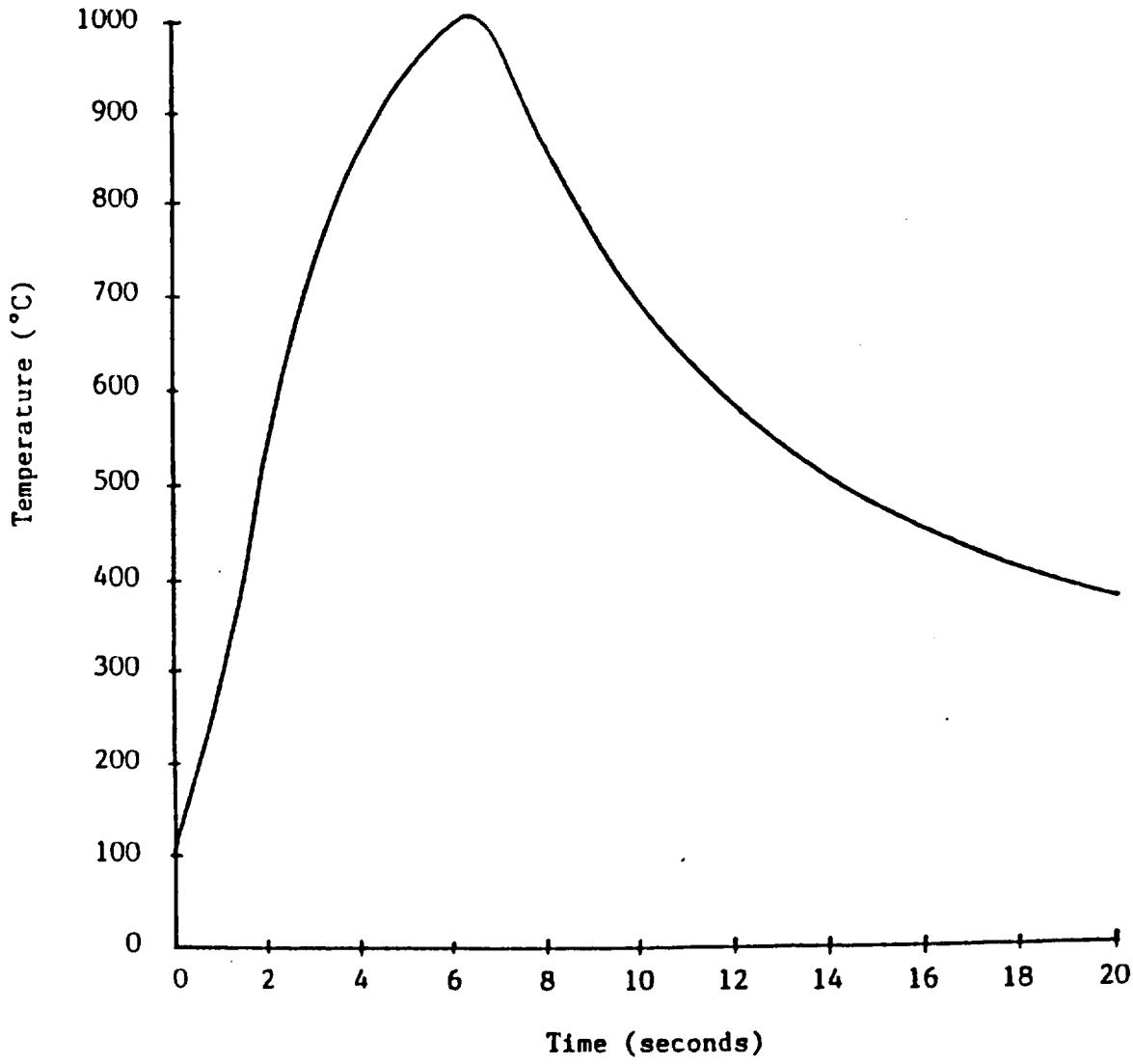


Figure 4.2-1) Flash Annealing Temperature versus Time Profile

4.3) MMIC Processing Sequence

A summary of the processing sequence for the MMICs fabricated under this program is shown in Table 4.3-1. The processing starts with properly prepared GaAs substrates.

Resistors can be implemented by either ion implantation or metalization. In the former case the FET implant doses or separate implants can also be used if a selective implant scheme is employed. Ohmic contacts and electrode metalizations are then formed at the same time as the FETs, and hence no additional processing steps are required.

For low inductance on-chip grounding, substrate via connections are used. Via holes are formed after the wafers have been thinned to the final thickness for standard MMICs, and possibly as thin as 2 mils for discrete power FETs. The backside of the wafer is then metalized for ease of die-attach and low thermal resistance. This also forms the ground plane for the RF circuitry in MMICs. Individual chips are obtained following dicing.

Table 4.3-1 MMIC Processing Sequence

1. Ion Implantation
2. Flash Annealing
3. Ohmic Contacts
4. Resistors
5. Gate Metalization
6. Overlay (First Layer) Metalization
7. Dielectric(s)
8. Additional Layer(s) Metalization
9. Wafer Thinning, Via Hole Etching, and Backside Metalization
10. Dicing

4.4) In Process Monitoring

The FETs and MMIC circuits are distributed across the wafer in a regular array, which is interrupted periodically by a "drop in" test pattern sparsely distributed across the wafer. This test pattern permits measurement and extraction of various materials and processing parameters at each stage of fabrication. These serve to monitor the process for deviations from nominal and hence eliminate further processing of any wafer with unacceptable expected final yield. Such practice is very important to ensure low chip costs in production of GaAs MMICs. A list of the test structures included in the standard test pattern used at MMInc. is provided in Table 4.4-1. In addition to this test pattern, FET structures representative of the devices used in the monolithic circuits are customarily included in the test areas on the wafer. These devices may be thoroughly characterized at DC / low frequency and subsequently measured at microwave frequencies to monitor actual device performance.

Table 4.4-1 Standard MMIC Test Pattern Structures

1. Large area diode for C/V characterization of the FET active layer.
2. 200 micron wide FET for DC/Low Frequency device characterization.
3. Sample resistors for each type of resistor fabricated, in each range of interest.
4. Sample capacitors for each type of capacitor fabricated, in each range of interest.
5. Sample Schottky diodes.
6. Hall mobility sample for each implanted layer.
7. Ohmic contact and sheet resistance test structure.
8. Test structure for contact resistance between the various metal layers.
9. A length of all thin metal layers for measurement of DC sheet resistance.
10. A "fat FET" test structure for drift mobility measurements.

5) RECEIVER FRONT-END MMIC COMPONENT CHARACTERIZATION

The approach in the design and fabrication of circuits at MMInc. is to take full advantage of computer modeling and analysis using the full extent of computer resources available. Toward this end all aspects of the circuit design and fabrication process has been modeled, including circuit responses, parasitic effects, mask layouts, interference coupling, doping profiles, via hole construction, FET equivalent circuit models, etc. In addition to this growing data base of design information; a sophisticated, proprietary software package has been developed to analyze and optimize the various characteristics that are somewhat unique to monolithic circuits. Because of the extensive analysis conducted on each circuit prior to fabrication, a high probability of success can be assured with very few iterations. This has been clearly demonstrated with the circuits developed under this program.

As each circuit is built, several built-in monitoring points are tested and evaluated during each step of the fabrication process. At each step measured data samples are taken and correlated with the computer model. This multi-step process assures that each wafer is made according to specification, and that the computer models are continuously updated. When new circuit elements or processing steps are introduced, computer models are updated and refined to reflect the characteristic performance of the final circuit.

Two types of testing are conducted on each circuit. The first type of testing is the in-processing tests designed to monitor and adjust the processing sequence. These tests are done using probes on a test pattern which is built into every wafer. Both DC and low frequency wafer measurements are used to monitor the fabrication process. This data is analyzed and compared with the original models such that predictions of the final chip characteristics can be made in the early processing stages of the wafer. The technique of using process monitoring data is an extremely valuable part of the manufacturing process at MMInc. not only because it allows prediction of the final

performance of the chips being processed, but also because it allows updating of the data base to maintain precise control of the fabrication process on all future wafers.

The second type of testing is the RF functional performance measurements. Although it may be possible to perform some of these measurement on wafer prior to slicing, this approach is generally not accepted as feasible for several reasons. First of all the equipment required to do wafer probe alignment, chip indexing, DC biasing and RF probing (especially at frequencies above 2 to 4 GHz) is extremely complicated and costly. Secondly, the RF responses may differ significantly when measured on a wafer using a probe than it would soldered down in a small package or in a sub-system. The reason for this is that the lead inductance and coupling capacitance would be different in a package than it would be for the probe. Most automatic RF probing requires coplanar input and output pads for low ground inductance, which is not available without extensive modifications for most microstrip circuits. Finally, wafer tests would not account for damage or stresses occurred during the dicing and packaging process.

5.1) MMIC TEST FIXTURING

As a practical matter, to prevent damage during RF testing the chips are soldered down on a gold plated subcarrier whose thermal expansion coefficient matches that of the GaAs. Kovar is a suitable subcarrier material, as it is a hard, stable material that will not bend easily and matches the thermal coefficient of expansion of the GaAs. As a conductor Kovar can be readily plated with copper and gold such that monolithic chips can be soldered to it with a suitable eutectic solder.

Several ceramic materials also have thermal expansion characteristics similar to GaAs. These include polycrystalline beryllium oxide, alumina monocrystalline silicon, quartz (a axis), and glass. Of these ceramics, alumina is used as an interface substrate not only because of its thermal expansion characteristics but also because it is good, low-loss microwave material that matches fairly well to the dielectric constant of GaAs.

The MMIC chips designed and fabricated in this program have been tested and characterized in a test fixture represented by the drawing shown in Figure 5.1-1. The fixture is designed in such a way that it can be used to test a wide variety of circuits of various sizes and configurations. It is built in three sections consisting of two end sections which house a microstrip to coax transition and a center section which contains the MMIC circuit chip. Since the fixture can handle various sized subcarriers, the subcarrier is not limited to testing just the MMIC circuits. Microstrip circuits can be tested in the subcarrier as well. One advantage of this fixture design is that it can be fully characterized on a microwave network analyzer. The significance of this is that the circuits can be measured inside the fixture and then the fixture characteristics can be mathematically de-embedded to reveal the true response of the device under test.

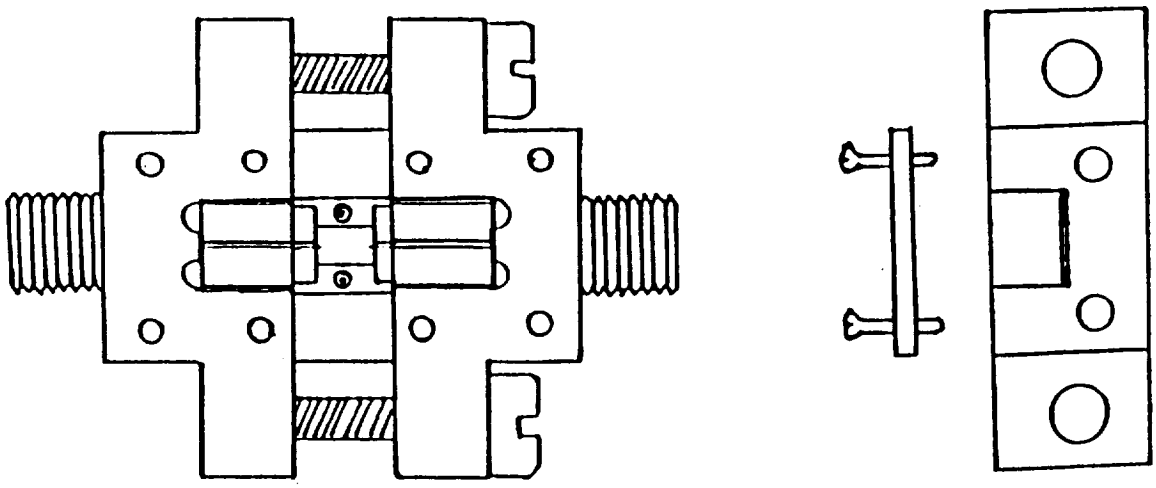


Figure 5.1-1) MMIC Test Fixture

5.2) RF MEASUREMENT SETUP

RF testing of two-port circuits (amplifiers) is performed on the HP 8410 vector network analyzer below 18 GHz, and on the PMI 1038-N10 scalar network analyzer to 26.5 GHz. The signal is provided by custom-designed 2 to 18 GHz and 2 to 26.5 GHz sweep frequency sources respectively. The source and the network analyzer are connected to a custom-built data acquisition system tied to a personal computer for local control which is in turn networked with a VAX-11/780-class supermicro computer for additional resources in data analysis.

Measurement on the dielectric stabilized oscillator is performed with the Tektronix 492 spectrum analyzer. Rough tuning of the monolithic LO chip / dielectric resonator assembly is performed on the network analyzer, with fine tuning and final characterization done on the spectrum analyzer. The mixer is also characterized with the spectrum analyzer using the sweep sources as RF and LO inputs respectively.

6) MEASURED PERFORMANCE OF MMIC COMPONENTS

The monolithic 20 GHz receiver front-end components described in section 3 have been fabricated using the techniques described in section 4. A photomicrograph of a completed GaAs wafer containing many 20 GHz receiver front-end MMIC chips is shown in Figure 6-1. A close-up photomicrograph of a fully monolithic "receiver-on-a-chip" is shown in Figure 6-2. The measured performance of the 20 GHz receiver front-end MMIC components, using the characterization techniques described in section 5, is presented in the following sections.

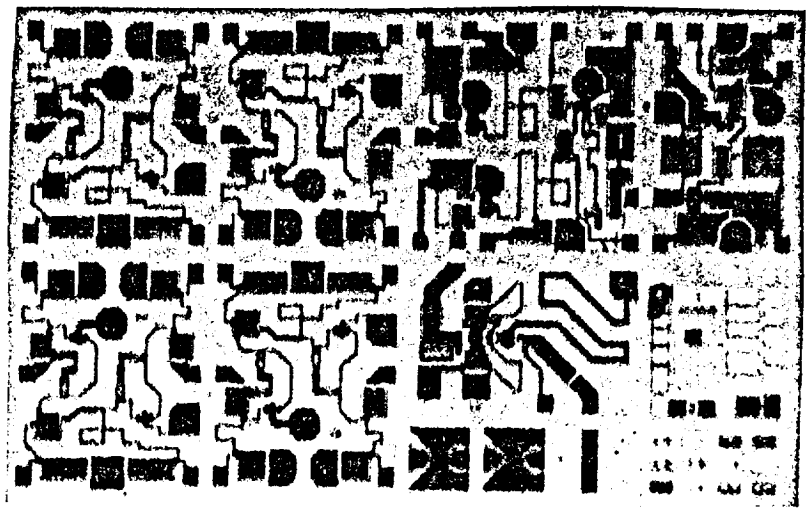


Figure 6-2) Photomicrograph of Fully Monolithic "Receiver-On-A-Chip"

6.1) LNA

As anticipated in the original proposal, a gate length of 0.5 microns or less is required for the FET device used in the LNA circuit. The fabrication equipment and techniques used at MMInc. are capable of reproducing these small dimensions. Considerable difficulties were, however, encountered in obtaining a suitable gate level mask from the vendor. Early masks delivered to MMInc. resulted in gate lengths in the 0.7 micron or larger range. As a result the measured gain of these early circuits was fairly low (in the several dB range) for the 2-stage chip. After delivery of an acceptable 0.5 micron gate mask, however, proper functionality was demonstrated as described below. As anticipated, fairly high yield has also been observed once the appropriate processing parameters have been "tweaked". This tends to support the premise that ultimately low cost production is an attainable goal. A detailed study of the yield factor is however beyond the scope of the present program.

As described in a previous section, the monolithic LNA consists of two cascaded (electrically connected on-wafer) identical circuits each with two FET stages. The original intend was to promote higher overall yield by permitting "mix and match" of the two sub-circuits. The yield of the final runs was, however, sufficient that such selection was not necessary. Hence entire cascaded (4-stage) LNA MMIC chips have successfully been RF tested as a single unit.

The gain response of a typical LNA chip mounted on a carrier is shown in Figure 6.1-1. The FETs were biased at the usual minimum noise region of I_{ds} = 15% I_{dss}. The data shown has <u>not</u> been unwound to the edge of the chip. Thus all fixture losses (approximately 1 dB) are still included in the result. As shown, a gain of 20 dB has been achieved in a single monolithic LNA chip over the designed band. Measured noise figure is about 6.9 dB at the high end of the band (21 GHz). This is somewhat higher than expected, but is not a major concern due to the masking effect of the hybrid first stage. It could probably be reduced somewhat in future design iterations.

MEASURED GAIN OF LNA

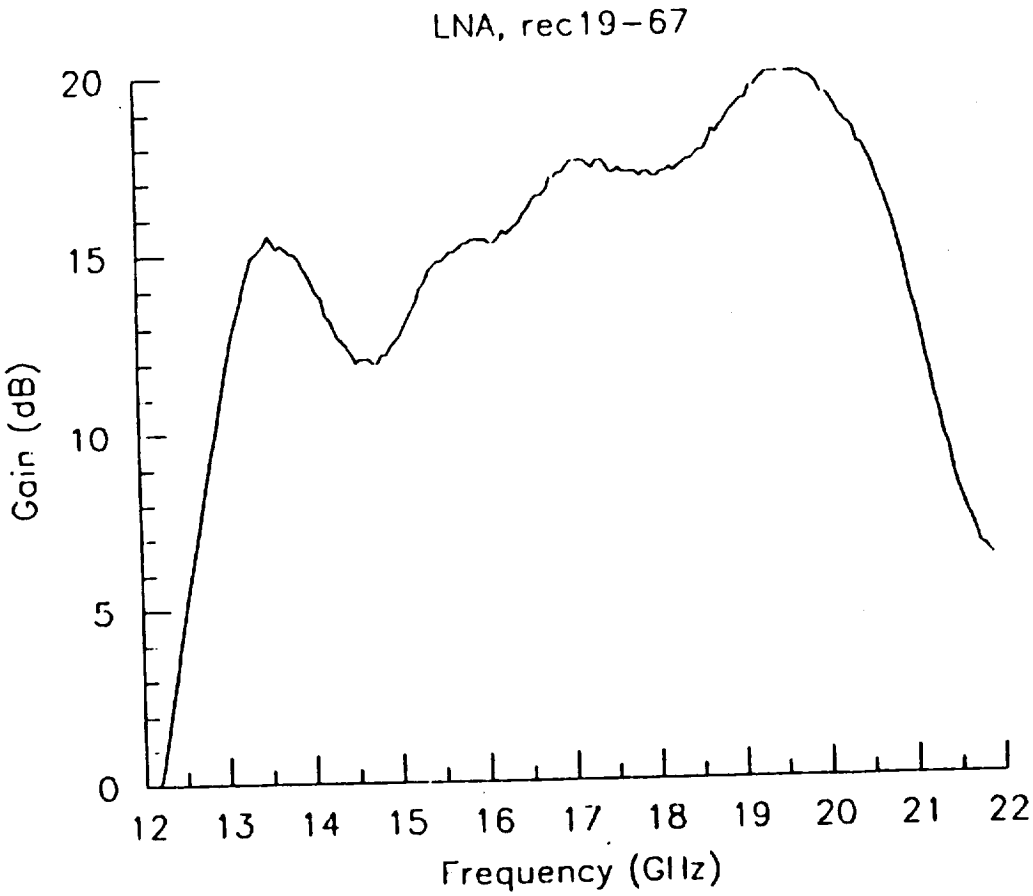


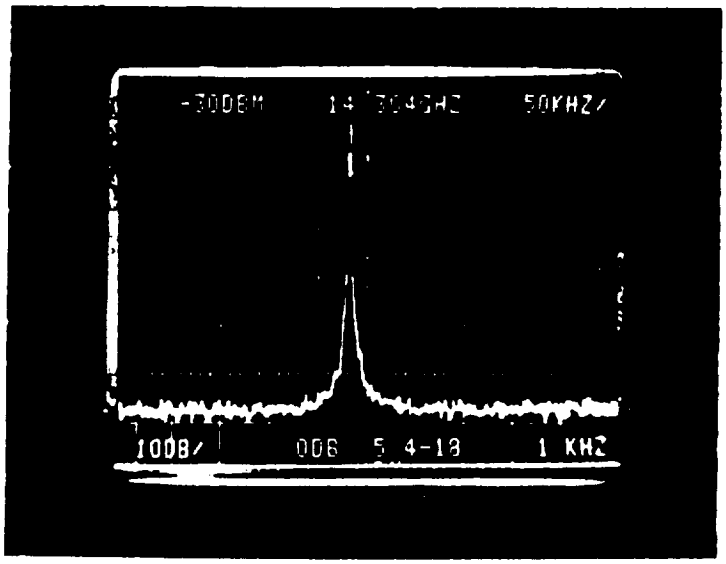
Figure 6.1-1) Measured Gain Response of MMIC LNA on Carrier

6.2) LO

The dielectric stabilized oscillator is characterized in an enclosed metallic housing which accommodates the MMIC oscillator chip and the dielectric resonator. The output of the assembled LO is displayed on the spectrum analyzer. A typical output spectrum (after "lock" to the dielectric resonator has been achieved) is shown in Figure 6.2-1. The apparent "width" of the signal is actually an artifact of the 1 KHz IF bandwidth of the spectrum analyzer utilized in this test.

The observed center frequency of the LO corresponds to the specified resonance of the dielectric resonator procured for this purpose. The measured negative resistance range of the DSO MMIC is actually quit wide as demonstrated by the frequency of the "free-running" oscillator with a reactive load on the resonator port. Oscillation frequencies between 13 GHz and 18 GHz have been obtained from this chip design by altering the reactive load, thus indicating that proper dielectric resonator selection would provide stable oscillations anywhere in this range. Measured output power of the unit delivered to NASA was -10 dBm, however this is not believed to be typical for this design. If necessary, however, output power could be increased in the next design iteration by adjusting the pull down resistor in the source follower stage of the on-chip buffer amplifier. Such a design iteration was, however, beyond the resources of the current program.

MEASURED OUTPUT SPECTRUM OF THE DSO



(SAMPLED THROUGH DIRECTIONAL-COUPLER)

Figure 6.2-1) Spectral Output of MMIC Dielectric Stabilized Oscillator

6.3) MXR/IFA

The mixer and IF amplifier portions of the MXR/IFA chip were characterized separately to ease data analysis. Since the inter-stage blocking capacitor was implemented on the mixer side, an external DC-block is required at the input of the separated IFA chip.

The mixer chip was tested using the two sweep sources and observing the appropriate product on the spectrum analyzer. Maximum mixing was observed when the gate voltages on the dual-gate FET were adjusted corresponding to maximum interaction of the control actions of the two gates. When the dual-gate FET was biased into more linear regions of the I-V characteristics, little mixing was observed. The level of the mixed product was however rather low. This has been attributed to a mismatch between the FET driver and the dual gate mixer on the monolithic chip. This mismatch can only be corrected via an additional mask iteration, which would be performed early in the next program phase. Since the modification involves only adjustment of the linear interface circuitry, however, it is not anticipated to present major problems.

The response of the IFA chip, mounted on carrier, has been measured from 2 to 6 GHz. A typical gain response curve is shown in Figure 6.3-1. A gain in excess of 14 dB has been observed over the 500 MHz IF bandwidth, which is in good agreement with prediction. The input and output return loss of the circuit is shown in Figure 6.3-2. Good match is obtained as expected from the common-source and common-drain stages. The location of the gain peak is slightly lower than anticipated, however this may be easily changed by adjusting the spiral inductor in the middle stage of the IFA.

MEASURED GAIN OF IF AMPLIFIER

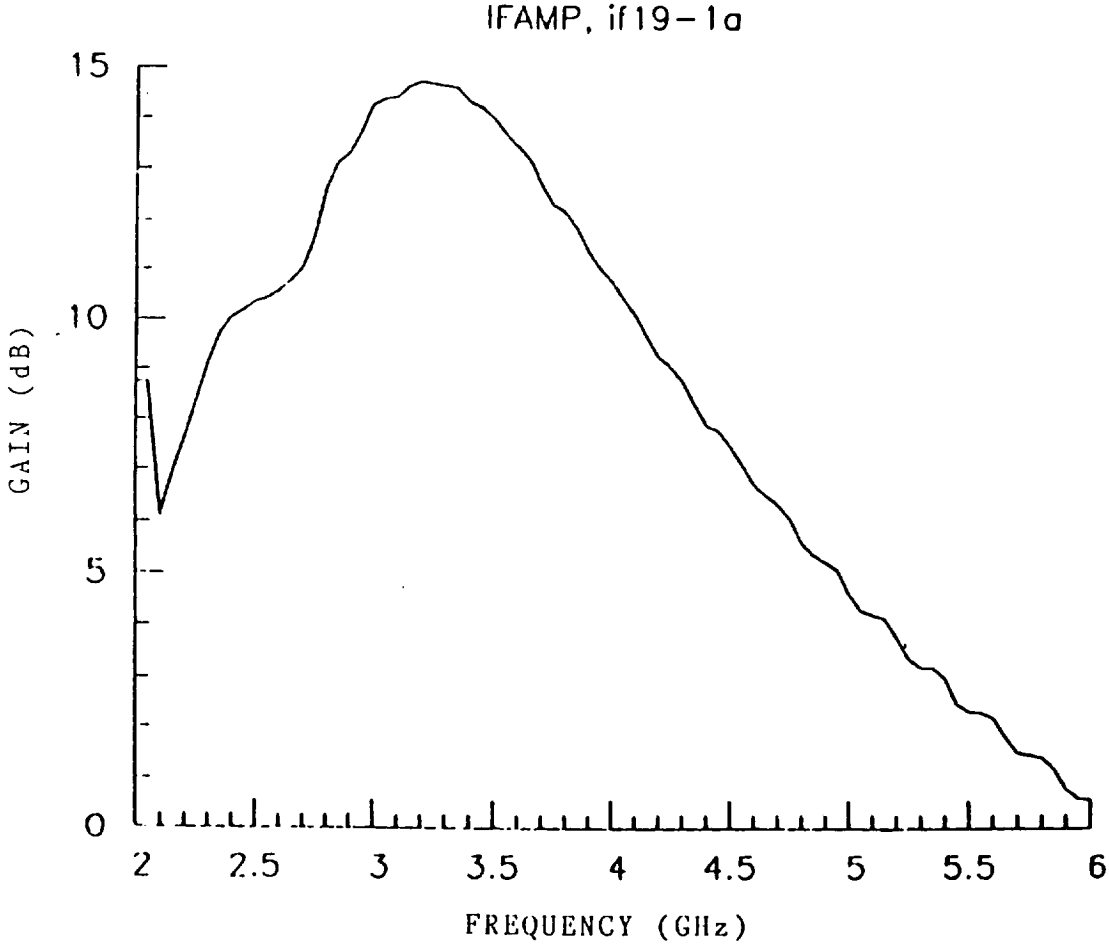


Figure 6.3-1) Measured Gain Response of MMIC IFA on Carrier

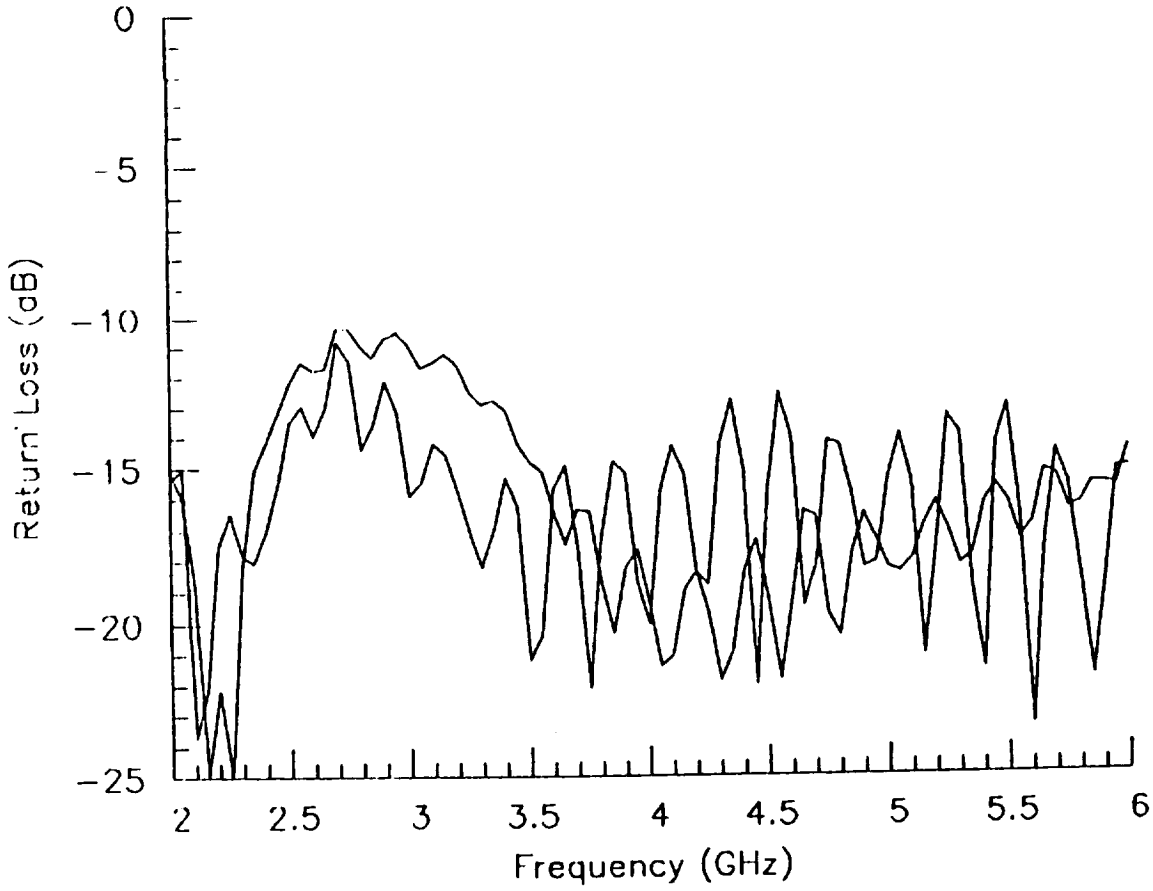


Figure 6.3-2) Input & Output Return Losses of MMIC IFA

6.4) SUMMARY OF MEASURED RESULTS

The receiver front-end monolithic components: the 20 GHz LNA, the dielectrically stabilized LO, and the mixer/IFA have been designed, fabricated, and tested. The function of these circuits have been verified by measurements. A summary of the results is shown in Table 6.4-1. Ample gain at 20 GHz has been achieved in the LNA monolithic circuit. The performance of the IFA is likewise close to expectation. A dielectrically stabilized oscillator has been successfully demonstrated using the LO monolithic circuit which also exhibits negative resistance over a wide range of frequency indicating the wideband applicability of the LO.

TABLE 6.4-1) Summary of Measured Performance of Receiver Front-End Chip Set

CIRCUIT	MEASURED PERFORMANCE	
LNA	Frequency Band:	17.7 to 20.2 GHz
	Gain:	19 $\pm$ 1.5 dB
	Noise Figure:	6.9 dB min.
DSO	Frequency:	14.3 GHz (set by Resonator)
	Negative Resistance Range:	13 to 18 GHz
	Output Power:	-10 dBm
MXR	Mixing Action OK over Entire LO and RF Band Conversion Gain Masked by Improper Interstage Matching	
IFA	Center Frequency:	3.3 GHz
	Gain over 500 MHz Band:	14.5 $\pm$ 0.5 dB

7) ESTIMATES OF HIGH-VOLUME PRODUCTION COSTS

The estimated costs of the monolithic receiver front-end component chips in high-volume production is basically the same as the presentation given in the proposal. Some adjustments are naturally necessary to account for updates in some costs such as GaAs materials since the field has matured considerably in the elapsed time. The cost per chip is also adjusted with respect to the final chip size. The updated results are provided in the following sections. An overall volume scaling factor, which has been widely used in the silicon industry, has been applied to the GaAs monolithics to arrive at an approximate cost for large scale production of MMIC receivers[6]. Since low cost production considerations are at the heart of this program, a closer examination of volume production costs is warranted and is therefore included in the following paragraphs.

Large Scale Production Cost Considerations of MMICs

The following cost projection assumes a production volume of two million (2×10^6) MMICs per year. The scaling factor can then be utilized to adjust this estimate to any moderately large production volume. This high-volume production will make possible the favorable GaAs chip fabrication yields typically associated with the learning curve scenario of semiconductor manufacturing. These projections assume non-recurring engineering costs of approximately $1M for complex circuits and approximately $500K or less for simpler ones.

For the baseline design MMIC chip, a total area of 9 mm^2 is assumed. Direct ion implantation process into 75 mm (3") diameter round slices of GaAs is assumed for the production line. A 20% d.c. probe yield is assumed for the active portion of the GaAs slice. This is equivalent to a 15% d.c. yield for the entire slice. A DC to RF yield of 75% is assumed. A 80% yield factor is used for the assembly and test with an overall yield of 12% (excluding slice edges) from start to finish with a 15% total RF probed chip yield. The overall yield is

achievable with the high production volumes of identical units and use of automated slice handling facilities. A start-up manufacturing cost of $250-500K will be incurred during the initial manufacturing phase. The overall yield then drops to the 6-9% level with the smaller volume circuit operations.

GaAs Substrate

Using the above assumptions of yield factors, the 2×10^6 circuits per year will require approximately 57,000-75mm (3") diameter GaAs wafers with 1140 slice starts per week. However, this is only a small volume when compared to the 30,000 to 50,000 slice starts per week capacity of a large-volume silicon I.C. manufacture.

State-of-the-art Liquid Encapsulated Czochralski (LEC) crystal pullers are capable of growing 3" diameter GaAs crystals to be centerless ground and cut into round slices of 0.025" thick. A generous yield factor of 50% for the material growth, slice preparation, and electrical qualification will modify the cost of qualified GaAs material to $\$4.68/in^2$ as an ultimate cost. However, for the 1988 time frame and considering the present state of development in GaAs crystal growth and wafer fabrication a substrate cost of $\$15.00/in^2$ will be more realistic.

Processing Labor and Direct Materials

Other direct materials costs through wafer "front-end" fabrication (up to wafer probe and dicing) are all individually small except for the cost of the gold metalization. The circuit "front-end" processing cost is estimated on a per slice basis using high throughput processing techniques compatible to the projected volume of 1140 slice starts per week. The ion implantation operation is assumed to be on a cassette-to-cassette basis with 3 implants per slice. The photolithography processing will include 0.5 micron geometries. The cost of the slice fabrications are shown in Table 7-1.

Table 7-1 MMIC Processing Cost per Slice

Ion Implantation	$ 9.60
Photolithography	$ 75.53
Vacuum metalizations	$ 6.40
Dielectric depositions	$ 2.67
Gold plating	$ 1.60
Pattern etching and formulations	$ 6.67
Dice sawing and chip separation	$ 16.00
Miscellaneous operations and inspections	$ 15.56
Total front-end processing cost	$134.03 per slice

D.C. and RF Probing

The d.c. testing is less costly since automated probing equipment can be utilized, assuming an average of 10 seconds per chip for the d.c. probing, 3 minutes RF probing with associated costs of $54.55 and $156.36 per slice. A summary of the projected cost per GaAs slice through the front-end processing area and probed is shown in Table 7-2.

Module Assembly

Components using MMIC chips will require only a few die attachments and wire bonds. If we assume a cost of $3.20 for the package and dielectric resonator, four minutes to adjust the LO frequency and final test the module, and an 80% yield factor the estimated cost of the receiver front-end comes to $19.30. The above cost estimate for an "average complexity" GaAs MMIC in volume production in the 1988 time frame assumes co-processing with telecommunications/commercial MMIC products to increase production volume. A captive DoD manufacturing facility will most probably increase the cost of device manufacturing. Cost estimates can be made with specific information on chip complexities and production volume.

Projected Costs of MMIC Components

Given the above background information the cost for the MMIC components for 10,000 downconverters can now be estimated. To use the above figures which were generated on the basis of 2 million MMICs per year, it is necessary to scale the figures using an appropriate scaling factor. Based on the industry wide experience in processing large scale silicon integrated circuits, each time the volume doubles the cost is reduced by 20 to 30 percent to a level of 70 to 80 percent of its original cost. For example, if the per unit cost of 5000 chips is $200, then the per unit cost of 10,000 chips is $140 to $160. Assuming the doubling cost factor is .707, then it can be said that the cost is

inversely proportional to the square root of the volume ratio; or $C_2=C_1(V_1/V_2)^{.5}$.

The total cost per system for the MMIC chips is estimated to be about $350.00 assuming 9 square mm per system, 7.5 percent yield, 10,000 production units and no initial set-up costs or NRE included.

Projected Costs of the Local Oscillator

The large scale production cost of the local oscillator (LO) depends largely on the cost of the dielectric resonator and the hybrid circuit that it is mounted on, since these components must be processed serially instead of in batch. Hence, there is a slight cost increase in the downconverter to cover the cost of the dielectric resonators and the labor associated with initial alignment. This cost amounts to approximately $40 in material and $8 in labor for high volume production.

Other Projected Costs

The housing is the next major cost component of the downconverter, second only to the monolithic circuits. The major factor contributing to its cost is the machining of the body and tapping the holes for the ridge waveguide transition and connectors. Since the monolithic chips will be soldered to a plated Kovar steel subcarrier, the housing can be made out of aluminum which is easy to machine without having to be concerned with thermal expansion interfaces with the GaAs. Consequently, all the machining can be one quickly, precisely and automatically on a tape-driven endmill. This includes the ridge transition and the cover lids as well. The tapping operation would have to be done by hand on a semi-automatic setup designed for speedy operation. The plating operation can be accomplished in large plating tank where several units can be plated at the same time. The entire finished housing would cost approximately $105 in large quantity

production of 10,000 units.

The remaining parts of the downconverter include connectors, cables, bias pins, subcarriers, the PC board, the waveguide window seal, and miscellaneous hardware (such as screws, etc.). All these components are considered high volume parts; that is, parts that are always manufactured in mass quantities of hundreds of thousands. The cost of these items is generally determined by the purchase quantity; hence, in lots of 10,000 the price should be small.

Consistent with high volume production the system has been configured to minimize all labor operations in assembly and testing. Nevertheless, there are a few operations that need to be done by hand and these include populate the subcarriers, assemble the housing, install the circuits in the housing, functionally test the circuits and system, inspect and package the system.

Populating the subcarriers takes approximately five minutes per carrier. The alumina substrates are first placed into position using an alignment fixture and then soldered using eutectic preforms. The MMIC chip is placed on the subcarrier next and soldered in place with a lower temperature preform. Bond wires are bonded down to interface the chip to the alumina subcarrier. Although this is a three step operation, enough of these can be done at a time so as to obtain an overall time of 5 minutes per carrier.

To assemble the housing, the ridge waveguide transition must be screwed into place and soldered down. The bias pins must then be soldered in as well. The RF and DC connectors and bias PC board must be installed. Finally, the subcarriers must all be installed and the RF and DC interconnections bonded in place. The entire operation takes less than 45 minutes including the installation of the circuits.

RF testing and fine tuning the LNA takes less than 30 minutes if only a single functional test is performed. It is assumed that this operation can be computer automated using an automatic spectrum

analyzer, a programmable source, and preset power supplies. Each RF subcarrier can also be checked prior to installation using a prepared fixture and setup, such that the subcarrier can be dropped in place and have the response measured with a "go/no go" indicator.

The remaining items of inspection, packaging, and supervision can be one in under 30 minutes provided that the data and records are kept track of by a computer.

Summary of Volume Production Costs

The total production costs of the two approaches are summarized in the Table 7-3. An estimated cost of $758 per receiver front-end represents a substantial cost savings from previously published estimates of several thousand dollars. The cost savings is a result of using microwave monolithic technology and utilizing dielectric stabilized FET oscillators in place of phase-locked multiplier chains for the LO source.

Table 7-3 Summary of Receiver Production Costs

Materials/Assemblies:	Cost
Housing	$105
Subcarriers	15
Connectors	20
Cable	85
Monolithic Chips	350
Dielectric Resonators	40
P.C. Board	35
Misc. Parts	20
Total Materials:	$670

Labor @$40/Hr.:

Task	M/H	Cost
Populate Subcarrier	.3	$ 12
Assemble Housing	.5	20
Integrate Circuits	.3	12
RF Testing/Tuning	.5	20
Inspection	.2	8
Package Unit	.2	8
Supervision	.1	4
Misc.	.1	4
Total Labor		$ 88

8) OPERATION AT ALTERNATE IF FREQUENCY

The two frequencies of interest in a receiver front-end (downconverter) are the RF frequency at the input and the IF frequency at the output. The LO frequency is automatically set once the RF and IF frequencies are decided; alternately, the IF frequency is set once the RF frequency and the RF-to-IF translation are decided. Of these two, the RF frequency range is determined by usage allocation and is therefore not a choice in practical situations. The 17.7 to 20.2 GHz RF band of this receiver front end falls into this category. The response of the monolithic LNA demonstrated in this program is nevertheless fairly wideband such that it might also find application in a number of other systems.

On the other hand, the IF frequency is usually chosen to suit the internal architecture of the communications system of interest. The 3.7 to 4.2 GHz range selected for the IF amplifier in this program was aimed at exploiting the ready availability of low cost additional hardware from existing TVRO applications. The final selection however remains flexible and will ultimately be determined by NASA.

The monolithic receiver front-end components demonstrated here have therefore also been assessed for operation at a different IF frequency range of particular interest to NASA. The specific frequencies considered are:

(a)	RF frequency range	19.2 to 20.2 GHz
(b)	RF-to-IF frequency translation	16.541 GHz
(c)	IF center frequency	3.373 GHz

The results are provided in the following sections.

8.1) DESIGN MODIFICATIONS

Since the desired RF frequency range is within the original band, the LNA design remains unaffected. This greatly reduces the risk associated with any future change of this type since the LNA is the most important component of the entire downconverter chain which sets key performance parameters such as the overall noise figure. The MMIC LNA chips demonstrated here is directly applicable to the alternate IF band specified.

On the other hand, the lower IF frequency may actually be of advantage since higher gain and lower noise figure are possible. The present MMIC IFA in fact exhibited a shift in response towards lower frequency. This can be easily modified to coincide exactly with the IF frequency range specified in the table above.

In the present LO design, the active device (FET) with appropriate feedback element presents a broadband negative resistance to the dielectric resonator which then sets the frequency of oscillation. Since the FET is capable of considerable gain in Ku band, there should be little difficulty to adjust the feedback element, which in this case is a single shorted stub to the source electrode of the FET, to "peak" the negative resistance to the neighborhood of the desired 16.541 GHz frequency. Of course a different dielectric resonator must also be utilized.

The last component to be considered is the mixer. In the present design, the RF port can remain unchanged. The LO port was originally designed for 14 to 16 GHz; hence a slight extension to 16.541 GHz should present no major difficulty. RF to LO isolation in the FET-driven mixer design is provided by the non-reciprocal nature of the device, and should not be affected by moving the frequencies slightly closer. The IF port incorporates a low-pass filter to reduce RF and LO leakthru. This should be insensitive to the lowering of IF frequency, but it may be advantageous to lower the cutoff frequency slightly.

8.2) PROJECTED PERFORMANCE

Based on the above considerations, the monolithic 20 GHz receiver front-end components demonstrated here: the LNA, LO, mixer, and IFA chips could be readily adapted to operate at an alternate IF frequency range if desired. The most critical component, the LNA, does not require any redesign. Only minor redesigns are needed for the remaining MMIC components. The changes involve changing the value of selected tuning elements which might be accomplished by changing only one level of mask. The performance of the redesigned chips in conjunction with the unchanged LNA chip is expected to be similar to those attained in the present program.

9) CONCLUSIONS AND RECOMMENDATIONS

In this phase II of a multi-phase program to develop a universal low cost 20 GHz receiver front end for advanced 20/30 GHz ground terminals, MMInc. has designed, fabricated, and characterized 1) a 20 GHz low noise GaAs MMIC amplifier, 2) a dielectrically stabilized local oscillator MMIC, and 3) a monolithic GaAs mixer / intermediate frequency amplifier. The excellent measured performance of these MMIC chips and their compatibility with MMInc.'s originally proposed receiver front end design approach has clearly demonstrated proof of concept for MMInc.'s low cost monolithic 20 GHz receiver front end. Although to date only R&D quantities of the MMICs have been fabricated, sufficient chips have been produced to ship five DC functional visually screened parts of each type to NASA. One of each was mounted on a custom carrier for RF data correlation, except for the DSO which was shipped in an enclosed housing with integral dielectric resonator to better demonstrate performance. Initial yields at MMInc. indicate that low production costs will be readily attainable and that higher levels of monolithic integration might also prove cost effective.

A gain of 20 dB has been achieved from the single chip monolithic LNA chip the full design band. The measured noise figure of 6.9 dB at the high end of the band is somewhat higher than expected, but is not a major concern due to the masking effect of the hybrid first stage. It could be reduced somewhat in a future design iteration if desired. Oscillation frequencies between 13 GHz and 18 GHz have been obtained from the monolithic DSO chip by altering the reactive load, thus indicating that proper dielectric resonator selection would provide stable oscillations anywhere in this range. Locking to a dielectric resonator has been demonstrated at 13.8 GHz. Measured output power of the unit delivered to NASA was -10 dBm, however this is not believed to be typical for this design. If necessary, however, output power could be increased by adjusting the pull down resistor in the source follower stage of the on-chip buffer amplifier. A gain in excess of 14 dB has been observed for the IF amplifier over the full 500 MHz IF bandwidth. The input and output VSWR were well below 2:1. The location of the gain

peak is slightly lower than anticipated, however this could be easily changed by adjusting the spiral inductor in the middle stage of the IFA. Such a change would also be necessary for operation at an alternate IF band if so directed by NASA. Maximum mixing action was observed in the monolithic mixer when the gate voltages on the dual-gate FET were adjusted corresponding to maximum interaction of the control actions of the two gates. The level of the mix product was however rather low. This has been attributed to a mismatch between the FET driver and the dual gate mixer on the monolithic chip. This mismatch can be corrected via an additional design iteration involving adjustment of the linear on-chip interface circuitry between the buffer amplifiers and the dual gate mixing FET.

The final set of design iterations described in this paragraph were beyond the resources of the current program, however they are relatively straightforward and are thus considered low risk compared to the progress already attained by MMInc. Between 75 and 80% of the chip set development effort has been completed. Since the higher risk aspects of the design have already been overcome, a low risk Phase III program consisting of a final MMIC design iteration followed by subsystems integration is recommended. As originally envisioned by MMInc., this phase III program would lead to completion of the hermetically sealed waveguide unit previously depicted in Figure 2-3. Completing development of this low cost unit, or a similar one optimized to an alternate IF band conforming to the ACTS high data rate experiments, would help realize the full potential of the next generation 20/30 GHz communications satellite technology.

10) REFERENCES

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TABLE A.2-1) Recommended Bias Conditions for MMIC Chips

CIRCUIT	BIAS CONDITIONS
LNA	V_d = 3 Volts V_g = -1.4 Volts (Adjust for Best Performance)
DSO	V_d = 4.5 Volts V_g = 0 Volts
MXR	$V_{d1} = V_{d4}$ = 3 Volts V_{ds} = 5 Volts $V_{g1} = V_{g4}$ = 0 Volts V_{g2} = 1 Volt (Adjust for Best Performance) V_{g3} = -1.5 Volts (Adjust for Best Performance)
IFA	$V_{d1} = V_{d2}$ = 5 Volts V_{g1} = -1.2 Volts (Adjust for Best Performance) V_{g3} = Self Biased (no connection)

All Circuits: External RF choke is recommended in series with each gate bias line (between the on-carrier 50 pF capacitors and the external power supply) to supress any potentially damaging parasitic low frequency (UHF) oscillations.

98-99

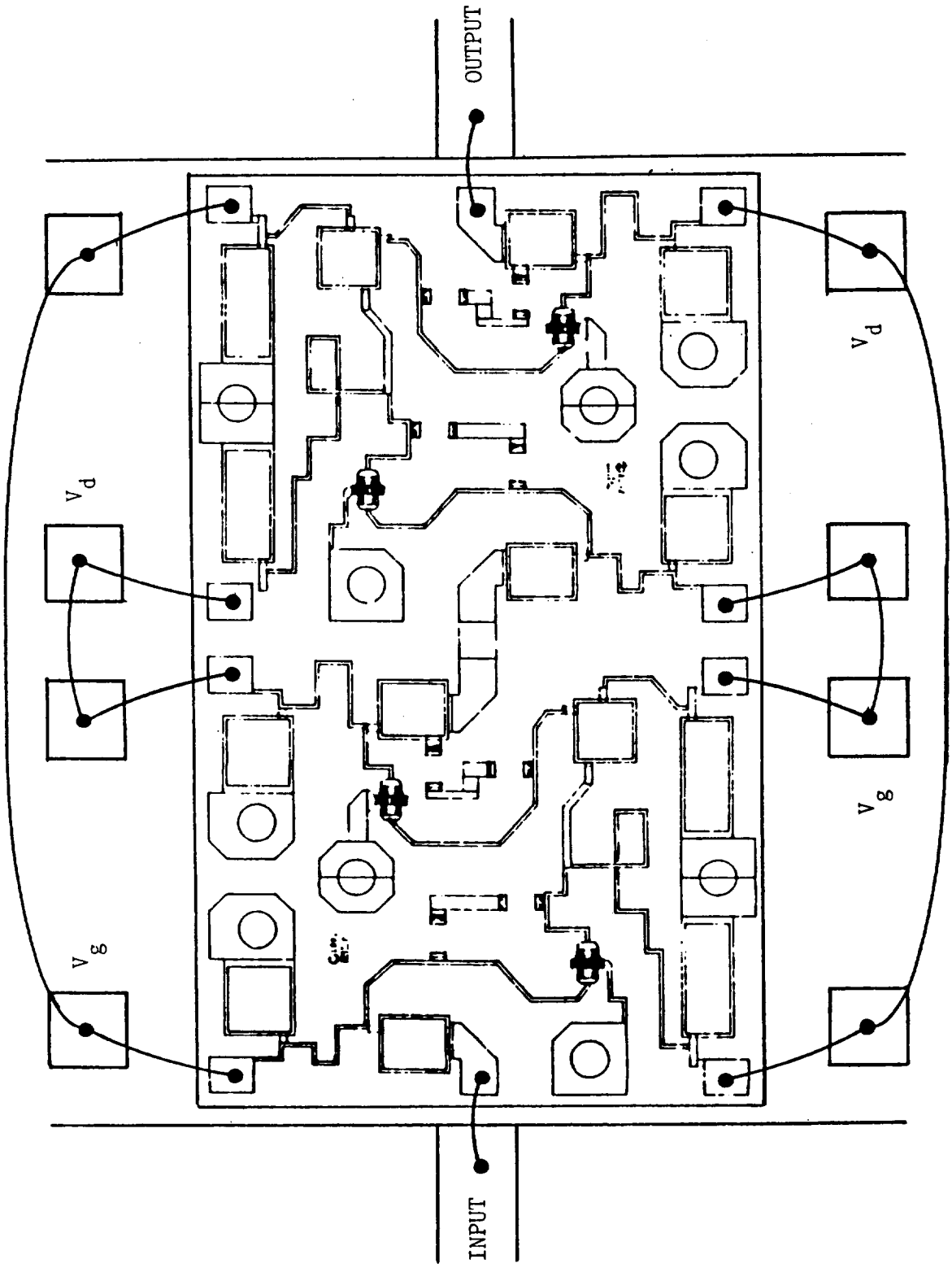

Figure A.2-1) DC Connections to MMIC Chips - (a) LNA

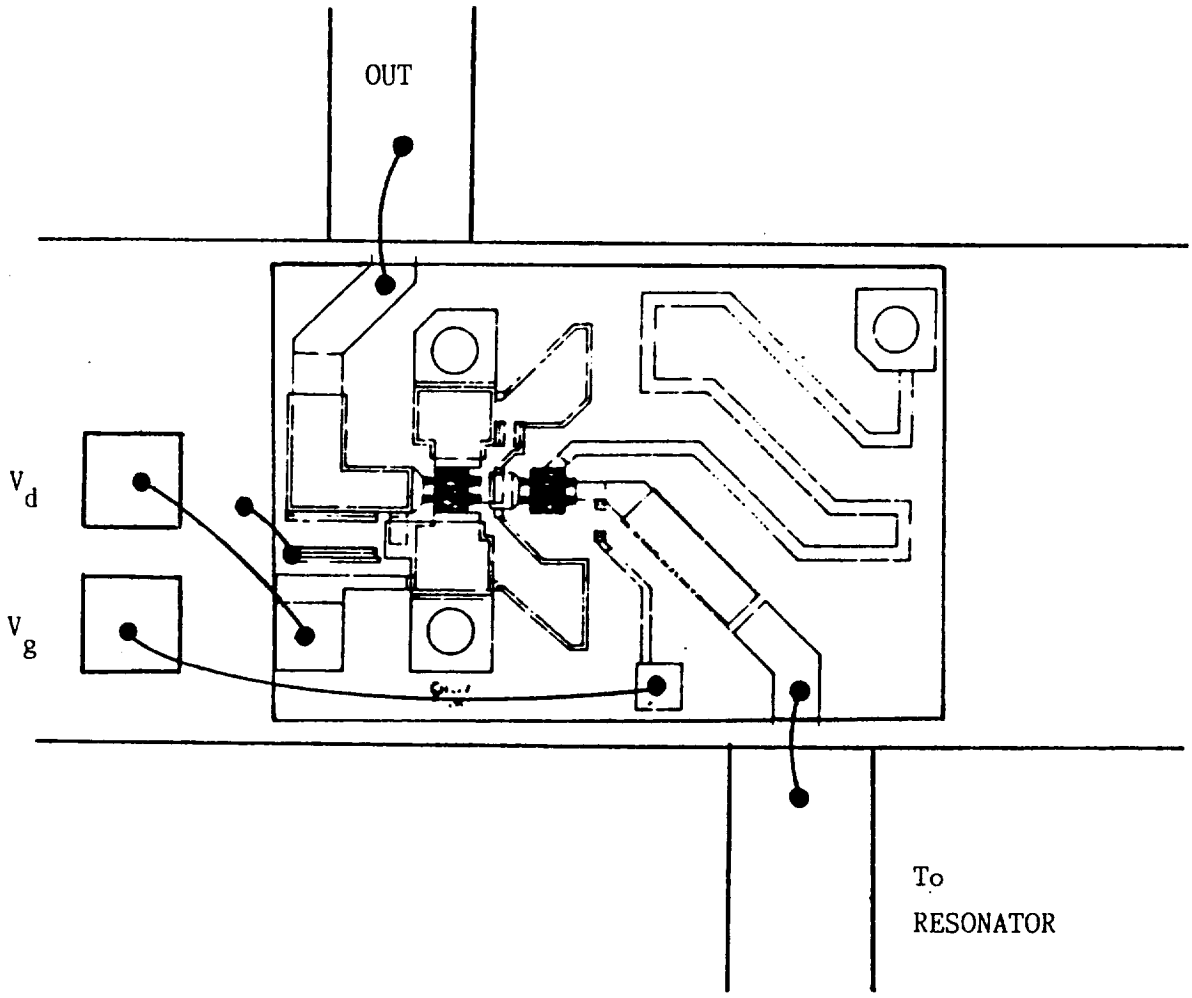

Figure A.2-1) DC Connections to MMIC Chips - (b) LO

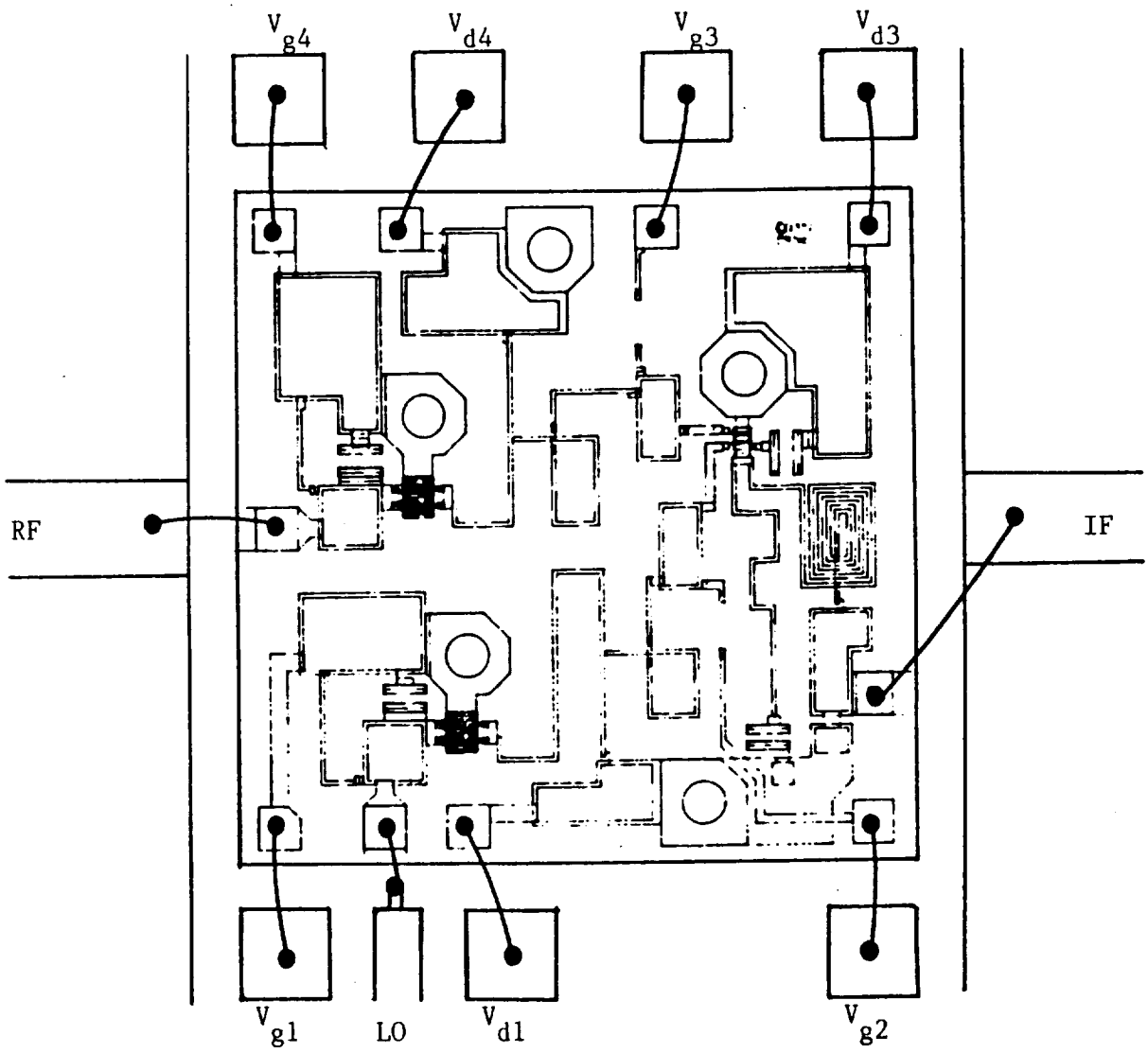

Figure A.2-1) DC Connections to MMIC Chips - (c) Mixer

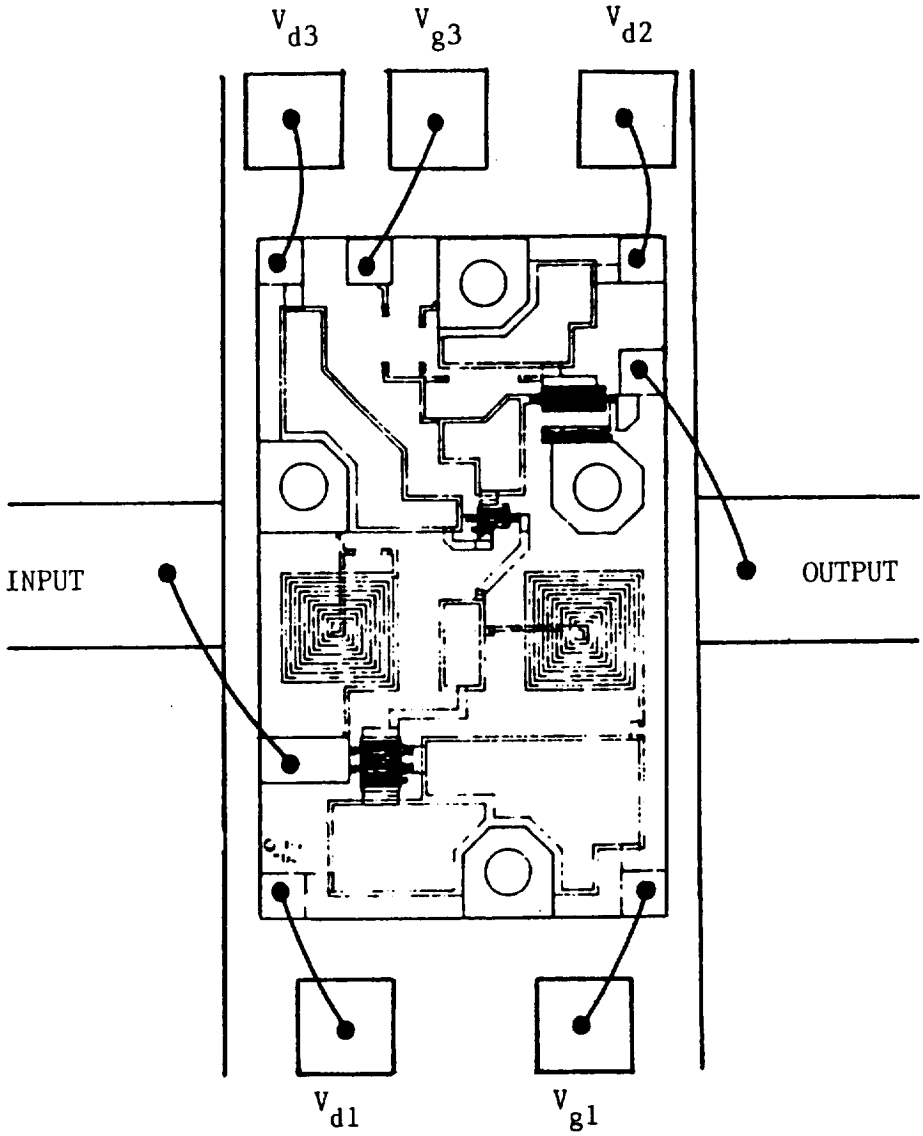

Figure A.2-1) DC Connections to MMIC Chips - (d) IFA